A Novel Method of Load Compensation Under Unbalanced and Distorted Voltages

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***Abstract*—In this paper, load compensation techniques under unbalanced and distorted voltages have been discussed. Two kinds of compensation methods are considered. In the first category, synchronous detection and modified equal current strategies are used under the unbalanced but sinusoidal source voltages. In the second method, load compensation based on instantaneous symmetrical component theory with positive sequence extraction is proposed and is shown to work under unbalanced and the non-sinusoidal source voltages. To support the proposed method, a 440 V (L-L) three-phase, four-wire distribution system is considered. The compensator is realized using a three-phase voltage source inverter (VSI) operated in the current control mode. Detailed digital simulation and experimental results are presented to validate the approach.**

***Index Terms*—Load compensation, unbalanced and distorted voltages, voltage source inverter.**

I. Introduction

A NUMBER of methods are available for unbalanced and nonlinear load compensation in the literature [1]–[5]. However these methods do not provide satisfactory compensation when the source voltages are unbalanced and distorted. Under these conditions, the synchronous detection methods provide a simple solution for the load compensation [6], [7]. These methods discuss load compensation for unbalanced and nonlinear loads supplied by source voltages that are unbalanced both in magnitude and phase.

In this paper, the synchronous detection methods are extended for load compensation under the unbalance in source voltages, with an additional freedom of setting a desired power factor of the source currents with respect to source voltages in the respective phases. However, the extended synchronous detection methods assume that the source voltages are sinusoidal. Another drawback of these methods is that they need synchronization for all three phases to generate reference currents. In general, using these methods, a zero sequence current flows even after compensation. Moreover the methods do not provide satisfactory compensation when the source voltages are unbalanced as well as distorted. For unbalanced and distorted waveform, one elegant method of load compensation based on extracting the active component of current is discussed in [8]. However in the final formulation of extracted reference current, the explicit setting of power factor is not apparent. The extraction of reference currents is computation intensive and involves the definition of various powers. On the other hand, the shunt algorithm based on generalized instantaneous reactive power theory [2]–[5], with input voltages as positive sequence voltages extracted using complex Fourier transform [9]–[11], provides satisfactory solution. The extraction of reference current based on instantaneous symmetrical component theory is simple and devoid of various definitions of the active and reactive powers [12]. Therefore, shunt algorithm for load compensation under unbalanced as well as distorted supply voltage based on instantaneous symmetrical component theory, along with the extraction of fundamental positive sequence voltage, is proposed in this paper. The formulation gives a freedom of setting the power factor of the source explicitly. Although, low pass filters can be used to remove the distortions in the source voltages and to feed them to shunt algorithm directly, it gives slow dynamic response of the compensator. The Fourier transform algorithm to extract the positive sequence voltages of the unbalanced and distorted source voltages ensures fast dynamic response of the compensator.

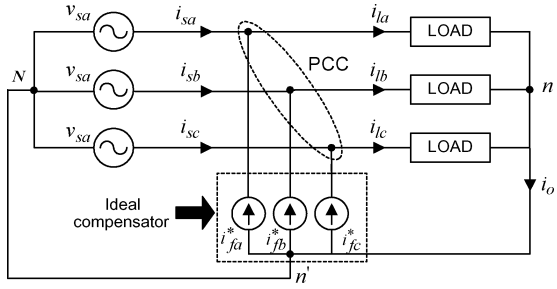

Fig. 1. Schematic diagram of a 3-phase 4-wire compensated system.

To illustrate this, a 440 V (L-L) three-phase, four-wire distribution system is considered. The schematic diagram of the system with the ideal compensator is shown in Fig. 1. The load and the compensator are connected at the point called point of common coupling (PCC). The system parameters given in Table I are considered for the simulation studies.

II. Direct Application of Shunt Algorithms

The reference compensator currents are extracted based on appropriate shunt algorithms [1]–[6]. The most established al-

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TABLE I
SYSTEM PARAMETERS

System voltage: 440 V (L-L) may contain unbalance and harmonics
Load: *R-L* unbalance load: Z_a=50 +j 0, Z_b=68+j32, Z_c=77+j62 Ω and three-phase full bridge diode rectifier supplying an output current of 4 A

gorithms for load compensation consider instantaneous reactive power theory, also known as p-q theory [1], generalized instantaneous reactive power theory [2], [5], theory of instantaneous symmetrical components [4]. The load compensation based on theory of instantaneous symmetrical components is much more simplified as compared to p-q theory. Also it allows the explicit setting of the power factor of the source. Based on this formulation, the reference currents for the compensator are given as [4]

$$i_{fa}^{*} = \frac{v_{sa} + \beta(v_{sb} - v_{sc})}{\sum_{j=a,b,c} v_{sj}^2}(P_{lavg} + P_{loss})$$
$$i_{fb}^{*} = \frac{v_{sb} + \beta(v_{sc} - v_{sa})}{\sum_{j=a,b,c} v_{sj}^2}(P_{lavg} + P_{loss})$$
$$i_{fc}^{*} = \frac{v_{sc} + \beta(v_{sa} - v_{sb})}{\sum_{j=a,b,c} v_{sj}^2}(P_{lavg} + P_{loss}) \quad (1)$$

where $\beta = \tan\phi/\sqrt{3}.$, ϕ is the desired phase angle between supply voltages (v_{sa}, v_{sb}, v_{sc}) and source line currents (i_{sa}, i_{sb}, i_{sc}) for the balanced system. For the unbalance voltages, ϕ is taken as phase angle between the positive sequence source voltages and the source currents in the respective phases. For unity power factor operation $\phi = 0$. The term P_{lavg} in (1) is the dc or mean value of the load power and is computed using a moving average filter that has an averaging time of half cycle or one cycle of supply voltage waveform depending upon whether load current contains odd or both odd and even harmonics. The term P_{loss} in (1) accounts for the losses in the voltage source inverter while realizing the actual compensator. With the ideal inverter given in Fig. 1, P_{loss} is equal to zero.

Initially, the supply voltage is considered to be balanced with an rms magnitude of 440 V (L-L) and the three-phase load consists of three different values of R-L combined with a three-phase full bridge diode rectifier, supplying an output current of 4 A as given in Table I. As a result of this, the load currents are unbalanced and nonlinear as shown in Fig. 2(a). For balanced sinusoidal source voltages, the algorithm (1) is now used to compute the reference compensator currents. The three-phase source currents are then computed by subtracting these reference compensator currents from the load currents in the respective phases. The compensated source currents are shown in Fig. 2(b). It can be seen from this figure that the source currents are balanced sinusoids and have unity power factor relationship with their respective phase voltages, as ϕ is set to zero in (1).

The source voltages are now assumed to be unbalanced but sinusoidal. The source voltages therefore can be expressed as

$$v_{sa} = V_{sma}\sin(\omega t)$$
$$v_{sb} = V_{smb}\sin(\omega t - 2\pi/3 + \theta_b)$$
$$v_{sc} = V_{smc}\sin(\omega t + 2\pi/3 + \theta_c). \quad (2)$$

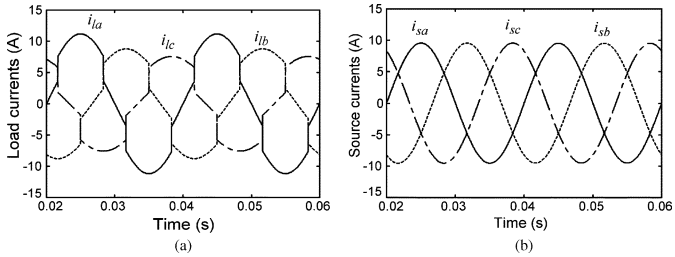

Fig. 2. (a) Unbalanced and nonlinear load currents. (b) Compensated source currents when the source is balanced.

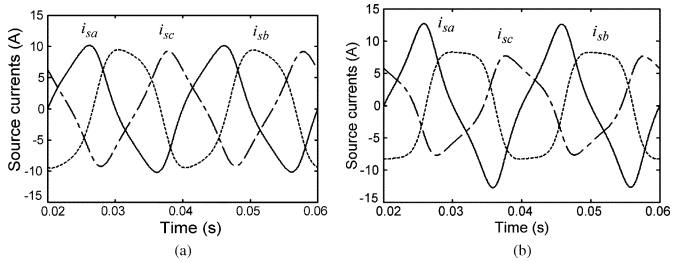

Fig. 3. Source currents with (a) magnitude unbalance and (b) magnitude and phase unbalance in source voltages.

In (2) V_{sma}, V_{smb} and V_{smc} are the peak values of source voltages in phase-a, b and c, respectively. The phase angles θ_b and θ_c account for the phase unbalance in phase-b and c voltages with respect to the phase-a voltage. The magnitude unbalance of 20% is considered such that $V_{sma} = 360$ V, $V_{smb} = 432$ V and $V_{smc} = 288$ V. There is no phase unbalance, i.e., both the angles θ_b and θ_c are equal to zero. For this case, the source currents are plotted in Fig. 3(a). It is evident from the figure that the source currents are unbalanced and distorted. In Fig. 3(b), in addition to magnitude unbalance as discussed above, unbalance in the phase angles with $\theta_b = 10^\circ$ and $\theta_c = -20^\circ$ is also considered. For this case, the currents become more unbalanced and distorted. The source currents after compensation become severely distorted, if the source voltages contain harmonics too. It is there felt that the use of shunt algorithm under the unbalanced and distorted supply voltage do not provide satisfactory compensation. In the following section, extended synchronous detection methods are discussed to overcome the above problem.

III. EXTENDED SYNCHRONOUS DETECTION METHODS

In [6] and [7], synchronous detection methods namely equal power criteria, equal current criteria and equal resistance criteria are discussed. In this, it is assumed that the source voltages have magnitude and phase unbalance without distortion. In this section, the above compensation methods are extended to facilitate the explicit setting of power factor in each phase. The unbalance source voltages are given by (2). The following criteria provide satisfactory load compensation under this condition.

A. Equal Current Criterion

Under this criterion, it is assumed that the source currents are equal in magnitude, i.e.,

$$I_{sma} = I_{smb} = I_{smc} = I_{sm} \quad (3)$$

where the subscript s denotes the source and the subscript m denotes the maximum or peak value. If it is desired that the source current should lag by ϕ radian in the respective phases, the instantaneous source currents are expressed as

$$\begin{aligned} i_{sa} &= I_{sma}\sin(\omega t - \phi) \\ i_{sb} &= I_{smb}\sin(\omega t - 2\pi/3 - \phi + \theta_b) \\ i_{sc} &= I_{smc}\sin(\omega t + 2\pi/3 - \phi + \theta_c). \end{aligned} \tag{4}$$

The average power supplied by the source, which is also average load power denoted by P_{lavg}, is given as

$$P_{lavg} = \frac{1}{2}(V_{sma}I_{sma} + V_{smb}I_{smb} + V_{smc}I_{smc})\cos\phi. \tag{5}$$

Using (3) and (5), we get

$$I_{sm} = \frac{2P_{lavg}}{\cos\phi \sum\limits_{i=a,b,c} V_{smi}}. \tag{6}$$

Therefore, the instantaneous source currents are given as

$$\begin{aligned} i_{sa} &= \frac{2P_{lavg}}{\cos\phi V_{sma} \sum\limits_{i=a,b,c} V_{smi}} v_{sa}\angle -\phi \\ i_{sb} &= \frac{2P_{lavg}}{\cos\phi V_{smb} \sum\limits_{i=a,b,c} V_{smi}} v_{sb}\angle -\phi \\ i_{sc} &= \frac{2P_{lavg}}{\cos\phi V_{smc} \sum\limits_{i=a,b,c} V_{smi}} v_{sc}\angle -\phi. \end{aligned} \tag{7}$$

In (7), the term $v_{sa}\angle -\phi$ is an instantaneous voltage that lags the instantaneous source voltage of phase-a, v_{sa}, by an angle ϕ and is generated by a delay circuit. Similar notations are used for phase b and c. The instantaneous reference currents for the compensator can be computed by subtracting source currents (7) from the load currents in the respective phases. These are expressed as

$$\begin{aligned} i^*_{fa} &= i_{la} - i_{sa} \\ i^*_{fb} &= i_{lb} - i_{sb} \\ i^*_{fc} &= i_{lc} - i_{sc}. \end{aligned} \tag{8}$$

B. Equal Power Criterion

In equal power criteria, the real power consumed in each phase after compensation is to be shared equally. Thus we have

$$P_a = P_b = P_c = P_{lavg}/3 \tag{9}$$

where P_a, P_b, and P_c are real power supplied by each phase, respectively. Using (2), (4) and (9), we get

$$\begin{aligned} \frac{1}{2}V_{sma}I_{sma}\cos\phi &= \frac{1}{2}V_{smb}I_{smb}\cos\phi \\ &= \frac{1}{2}V_{smc}I_{smc}\cos\phi \\ &= P_{lavg}/3. \end{aligned} \tag{10}$$

Therefore, the peak of source current in respective phases after compensation is given as

$$I_{smj} = \frac{2P_{lavg}}{3\cos\phi V_{smj}} \quad \text{for } j = a, b, c. \tag{11}$$

Instantaneous source currents can be expressed as

$$i_{sj} = \frac{2P_{lavg}}{3\cos\phi V^2_{smj}} v_{sj}\angle -\phi \quad \text{for } j = a, b, c. \tag{12}$$

The instantaneous reference compensator currents are computed using (8).

C. Equal Impedance Criterion

In the equal impedance criterion, the source should see the same impedance in each phase after compensation. With this assumption, we have

$$Z_a = Z_b = Z_c = Z. \tag{13}$$

Therefore

$$\frac{V_{sma}}{I_{sma}} = \frac{V_{smb}}{I_{smb}} = \frac{V_{smc}}{I_{smc}} = |Z|. \tag{14}$$

Substituting I_{sma}, I_{smb}, and I_{smc} from (14) in (5), we get

$$|Z| = \frac{\sum\limits_{i=a,b,c} V^2_{smi}}{2P_{lavg}}\cos\phi. \tag{15}$$

Therefore, the compensated source currents are given as

$$i_{sj} = \frac{2P_{lavg}}{\cos\phi \sum\limits_{i=a,b,c} V^2_{smi}} v_{sj}\angle -\phi \quad \text{for } j = a, b, c. \tag{16}$$

The reference compensator currents are computed using (8).

In all the above three methods of the compensation, the phase unbalance in compensated source currents can not be removed, therefore the neutral wire will always carry some current. However, if the source voltages have phase balance, only then the equal current strategy will make neutral wire to carry zero current. In the following section we give a modified equal current strategy, which gives completely balanced and sinusoidal source currents irrespective of unbalance in magnitude and phase angles.

D. Modified Equal Current Strategy

Let there be unbalance in magnitudes and in phase angles of the source voltages as given by (2). Let the fictitious set of three-phase voltages be balanced and are given by

$$\begin{aligned} v'_{sa} &= V'_{sm}\sin\omega t \\ v'_{sb} &= V'_{sm}\sin(\omega t - 2\pi/3) \\ v'_{sc} &= V'_{sm}\sin(\omega t + 2\pi/3). \end{aligned} \tag{17}$$

The use of balanced voltages in the algorithm produces balanced compensated source currents. For balanced compensated source

currents, both sets of voltages given by (2) and (17) should yield equal average load power, P_{lavg}. Due to this, the equal current criterion (3) is valid. From this requirement, we obtain

$$\frac{3}{2}I_{sm}V'_{sm}\cos\phi = \frac{1}{2}\left(V_{sma}I_{sm}\cos\phi + V_{smb}I_{sm}\cos(\phi+\theta_b) + V_{smc}I_{sm}\cos(\phi+\theta_c)\right). \quad (18)$$

Therefore, we have

$$V'_{sm} = \frac{1}{3}(V_{sma} + V_{smb}\alpha_b + V_{smc}\alpha_c). \quad (19)$$

In the above equation

$$\alpha_b = \frac{\cos(\phi+\theta_b)}{\cos\phi} \text{ and } \alpha_c = \frac{\cos(\phi+\theta_c)}{\cos\phi} \quad (20)$$

and ϕ is the desired phase angle between the source voltage v_{sa} and the compensated source current i_{sa}. In case of the unbalance magnitudes only, the angles $\theta_b = \theta_c = 0$, the factors α_b, and α_c in (20) reduce to unity. Consequently, the term, V'_{sm} in (19) is the average of the unequal magnitudes V_{sma}, V_{smb} and V_{smc}. Once V'_{sm} is known, the instantaneous voltages v'_{sa}, v'_{sb} and v'_{sc} are computed using (17) by using time synchronization with source phase-a voltage. The phase-b and c voltages i.e., v'_{sb} and v'_{sc} can be derived from v'_{sa} by phase shift of $-120°$ and $120°$, respectively. Thus only phase-a synchronization is needed. This is another advantage over extended synchronous detection methods [6], [7], where synchronization is required for all three-phases. These source voltages are then used in (1) to compute the compensator reference currents. This method provides a simple formulation for generation of the reference currents. The source currents thus obtained will be sinusoidal and balanced irrespective of the unbalance in source voltages.

The above algorithm may be referred as Modified Equal Current Strategy. Similar strategies have been reported as Sinusoidal Current Source Strategy in [13] and Equal Current Criteria in [6], [7]. However in [13], to find the fictitious balanced set of voltages for control algorithm, the complex $\alpha - \beta - 0$ transformations and elaborate computations are required. In [6], [7], the synchronous detection method is used but it is limited to the case of unity power factor and magnitude unbalance only in order to carry zero neutral current. The modified algorithm given above, using algorithm (1) is simple and considers unbalances in magnitudes and/or phase angles. The algorithm also provides the facility of setting the desired power factor angle, ϕ.

It is to be noted that if we consider the fictitious balanced supply voltages v'_{sa}, v'_{sb}, and v'_{sc}, then these would supply only average load power without zero mean oscillating active and reactive powers. Since the actual supply has unbalance, the source supplies some zero mean oscillating active and reactive powers.

All above methods are suitable when the source voltages are unbalanced in magnitudes and phase angles but are not distorted. For the source voltages under distortion, a scheme based on instantaneous symmetrical component theory and extraction of positive sequence of source voltages at the point of common coupling is proposed in the following section.

E. Using Shunt Algorithm With Positive Sequence Extraction of Source Voltages

When the source voltages are distorted, they can no longer be directly fed to the shunt algorithm as illustrated in Section II. To improve the performance of the algorithm, balanced three-phase voltages are to be fed as input voltages to the algorithm. Therefore, positive sequence components of terminal voltages are extracted using the power-invariant instantaneous symmetrical component transformation [9]–[11]. This is given by

$$\boldsymbol{v}_{sa012} = \begin{bmatrix} v_{sa0} \\ v_{sa1} \\ v_{sa2} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \quad (21)$$

where $a = e^{j120°}$ is a complex operator and v_{sa012} is a column vector with instantaneous zero, positive and negative sequence voltages as its elements. Let us now define the phasor zero, positive and negative sequence voltages as $\boldsymbol{V}_{sa0}$, $\boldsymbol{V}_{sa1}$, and $\boldsymbol{V}_{sa2}$, respectively. Defining a column vector as

$$\boldsymbol{V}^t_{sa012} = [\boldsymbol{V}_{sa0} \quad \boldsymbol{V}_{sa1} \quad \boldsymbol{V}_{sa2}]$$

the following equation is used to obtain the symmetrical components [9]–[11]:

$$\boldsymbol{V}_{sa012} = \frac{\sqrt{2}}{T}\int_{t_1}^{t_1+T} \boldsymbol{v}_{sa012}e^{-j(\omega t - 90°)}dt \quad (22)$$

where t_1 is any instant and T is the duration of one cycle of supply voltage assuming that the supply voltages may have odd as well as even harmonics. The integral is computed through a moving average filter to have fast dynamic response as compared to conventional low pass filter. Let the voltage of phase-a in phasor form be given by $\boldsymbol{V}_{sa1} = |\boldsymbol{V}_{sa1}|\langle\phi_{sa1}$. Then, the instantaneous reference voltage of phase-a will be as follows:

$$v_{sa1} = \sqrt{2}|\boldsymbol{V}_{sa1}|\sin(\omega t + \phi_{sa1}). \quad (23)$$

The other two phase voltages v_{sb1} and v_{sc1} can be obtained from phase-a voltage, v_{sa1} by phase shift of $-120°$, and $120°$, respectively. The shunt algorithm (1) is now fed with only the positive sequence voltages of the distorted source voltages for the reference current generation. As a result of this, the compensated source currents become balanced and sinusoidal.

IV. Simulation Studies

The compensator topology chosen for simulation as well as experimental study is the neutral clamped inverter circuit as shown in Fig. 4. It consists of two dc storage capacitors of the same rating and a three-phase voltage source inverter. Each leg of the inverter has two insulated-gate bipolar transistor (IGBT) switches with antiparallel diodes across them. In this circuit, the junction n' of the capacitors is connected to the neutral point of the load. The clamped neutral allows a path for the zero sequence current and therefore three currents can be independently controlled. The computed reference compensator currents (i^*_{fa}, i^*_{fb} and i^*_{fc}) in the methods discussed above are tracked by using a VSI in a hysteresis band current control. The

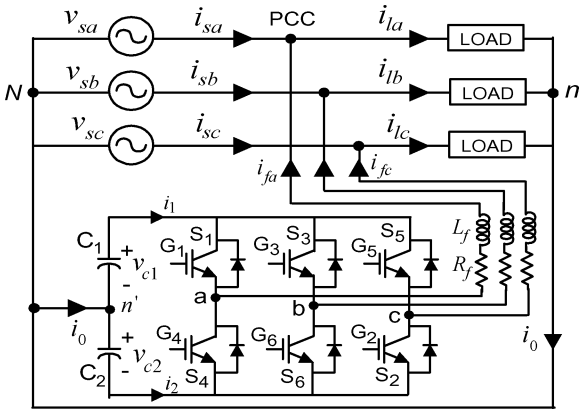

Fig. 4. Three-phase, four-wire compensated system with actual compensator.

TABLE II
COMPENSATOR PARAMETERS

DC capacitors (C_1 , C_2): 2000 μF each
Interface inductors (L_{fa}, L_{fb}, L_{fc}): 20 mH, 0.2 Ω
Reference voltage for each dc capacitor: 600 V
Hysteresis band for current = 0.2 A

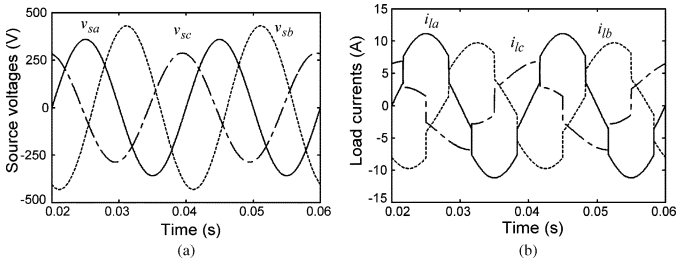

Fig. 5. (a) Unbalanced source voltages. (b) Load currents.

system parameters are same as given in Table I. The compensator parameters are given in Table II.

The above concepts are validated through simulation studies with ideal compensator and with the actual compensator circuit. The unbalanced source voltages with respect to magnitudes and phase angles are shown in Fig. 5(a). The peak voltages of phases a, b, and c are 360, 432, and 288 V, respectively. The phase unbalance in phases b and c are 10° and $-20°$, respectively. With these source voltages, the load currents are depicted in Fig. 5(b). It is seen from this figure that the load currents are unbalanced and nonlinear due to unbalanced R-L load and three-phase full bridge diode rectifier load.

For the equal current criterion, discussed in Section III-A, the compensated source currents are shown in Fig. 6. The voltage scale in the figure is reduced by a factor of 20 to bring the two waveforms in the same scale (to get the actual voltage, it has to be multiplied by 20). This allows easy comparison of the phase angle between voltage and current in the same phase. It is evident from this figure that the compensated source currents are equal in magnitude but their phase angles have same unbalance as the source voltages. The phase angle between voltage and compensated source current in phase-a is set to be 24°, which is also seen from the figure.

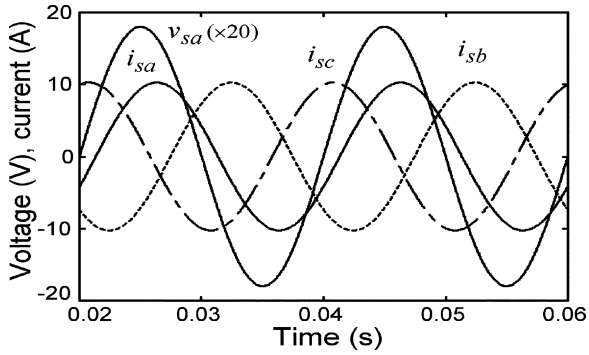

Fig. 6. Compensated source currents for equal current strategy.

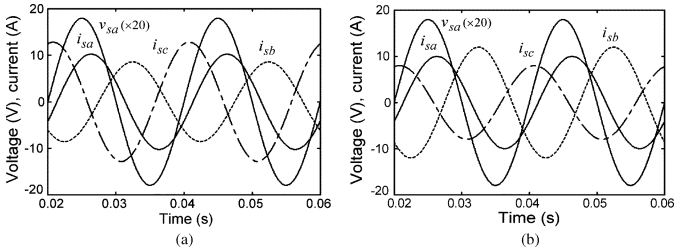

Fig. 7. (a) Compensated source currents for equal power strategy. (b) Compensated source currents for equal impedance strategy.

For the equal power criterion, the source currents are given as per (12). The reference compensator currents are computed using (8). The source currents are plotted in Fig. 7(a). It is observed that the source currents are unbalanced but sinusoidal. For the source current in phase-a, a power factor of 0.91 lagging (24°) is desired with respect to voltage in phase-a. This can also be seen from Fig. 7(a).

Compensated source currents for the equal impedance criterion are computed using (16) and the reference compensator currents are estimated as per (8). The compensated source currents are shown in Fig. 7(b).

When the modified equal current strategy is employed, the compensator gives better performance as compared to the previous methods. The (1) is employed for extracting the compensator reference currents. In (1) the terms v_{sa}, v_{sb} and v_{sc} are replaced by v'_{sa}, v'_{sb}, and v'_{sc}, respectively. These voltages are computed as discussed in Section III-D. The source voltage in phase-a and compensated source currents in phases a, b and c are given in Fig. 8(a). A power factor of 0.91 lag is set for source voltage and current in phase-a. The source voltage and current waveforms for unity power factor in phase-a are shown in Fig. 8(b). The currents in phase-b and c are also given in the figure. It is seen that the source currents are balanced and sinusoidal and hence no zero sequence current flows in the neutral wire. The equal current compensation method based on the synchronous detection method of [6]–[8] cannot compensate for the zero sequence current and hence it flows into the system through the neutral wire. This happens because compensated source currents have phase unbalance due to the phase unbalance in the source voltages.

When the source voltages are distorted the above formulations do not work as explained in Section III-E. Under distorted source voltage conditions, we extract their positive sequence

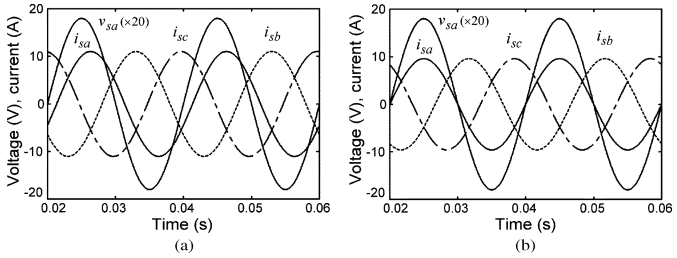

Fig. 8. Compensated source current with modified equal current strategy (a) at power factor 0.91 lag in phase-a (b) at unity power factor in phase-a.

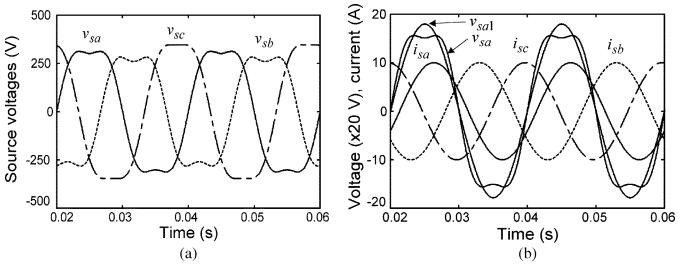

Fig. 9. (a) Distorted source voltages. (b) Phase-ya source voltage and compensated source currents for $\phi = 24°$.

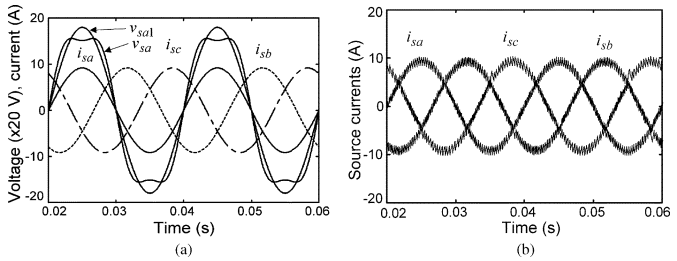

Fig. 10. Compensated source currents with fundamental extraction of distorted source voltages (a) at unity power in phase-a ($\phi = 24°$) (b) compensated source currents with real inverter circuit.

voltage. These voltages are then fed to the shunt algorithm (1) to extract compensator reference currents. The distorted source voltages are shown in Fig. 9(a). The fundamentals of the voltages have an unbalance of $\pm 10\%$. The total harmonic distortions in phase-a, b, and c are 16%, 18%, and 14%, respectively. The compensated source currents, distorted source voltage, and its fundamental are plotted in Fig. 9(b). It is also seen from the figure that the source currents are balanced and sinusoidal even when the source voltages are unbalanced and distorted. For unity power factor in phase-a, the source currents are illustrated in Fig. 10(a). The compensated source currents with voltage source inverter circuit given in Fig. 4 are plotted in Fig. 10(b). The source currents in the figure also contain inverter switching frequency components and notches. The notches in the current waveforms are due to the finite value of the interface inductance.

V. Experimental Results

The prototype compensator model given in Fig. 4 is developed in the laboratory. The voltage and current signals in the power circuit are sensed using Hall effect voltage and current transducers. For synchronization a clock is derived from phase-a source voltage. An IBM compatible PC acquires these signals through analog-to-digital converter (ADC) channels of a data-acquisition card PCI 9118DG. Based on these quantities, the program written in C/C++ for the shunt algorithm as discussed in Section III-E is implemented. The program computes instantaneous reference currents for the compensator. These reference currents are converted to analog values through three DACs.

TABLE III
System Parameters for Experimental Setup

System voltage: 100 V peak, 50 Hz
Load: Z_a = 49 + j 20 Ω, Z_b = 96 + j 0 Ω, Z_c = 161 + j 85 Ω. Three-phase full bridge diode rectifier drawing dc load current of 0.625 A
DC capacitors (C_1 , C_2)**:** 2000 μF each
Interface inductors (L_{fa}, L_{fb}, L_{fc})**:** 40 mH, 2 Ω
PI controller gains: K_P = 10, K_i=1
Reference voltage for each capacitor: $V_{dc\,ref}$=130 V
Hysteresis band: ± 0.2 A

The actual compensator quantities are obtained using Hall effect voltage and current transducers. The two currents in each phase are compared and the logic signal and its complementary signal are generated. These logic signals are given to a blanking circuit to create dead time in order to avoid short circuit during the ON-OFF transition state of the two switches (i.e., S_1 and S_4 in Fig. 4) on the same leg of the inverter. The above is also referred as PWM controller. The output signals from the PWM controller act as input signals to the driver circuit of the IGBT. The gate drive circuit of the IGBTs is supplied by an isolated supply. The dc voltages v_{c1} and v_{c2} (in Fig. 4) for the inverter are regulated to their reference value using PI controller. The dc power supply provides required dc voltage levels to the PWM control circuit.

The parameters for 3-phase, 4-wire compensated system are given in Table III. The experiments are performed at 100 V level. The magnitude unbalance in source voltages is created using dimmer-stat and phase unbalance is achieved using phase shifter. The unbalance in phase voltages is such that the peaks of the source voltages are 80, 100, and 65 V in phases a, b, and c, respectively, as shown in Fig. 11(a). In addition to this, phase-b voltage has a phase angle unbalance of $-30°$. It is seen from this figure that supply voltages are not perfectly sinusoids. The load currents at these voltages are depicted in Fig. 11(b). As observed from the figure, the load current waveforms are unbalanced and have nonlinearity due to the rectifier load. Fig. 11(c) depicts the compensated source currents when (1) is used. These results are similar to simulation results, given in Fig. 3(b). It is observed from this figure that the direct application of control algorithm (1) results into unbalanced and distorted source currents and, therefore, it is not a satisfactory solution.

The reference compensator currents are now extracted using (1) with positive sequence voltages. The positive sequence voltages have been computed in real time using algorithm discussed in Section III-E. While reconstructing positive sequence voltages in time domain, the synchronization has been done in the software. Based on this modified algorithm, the compensated source currents with ideal inverter are shown in Fig. 11(d). These are perfectly balanced and sinusoidal and are in phase with their positive sequence voltages. When voltage

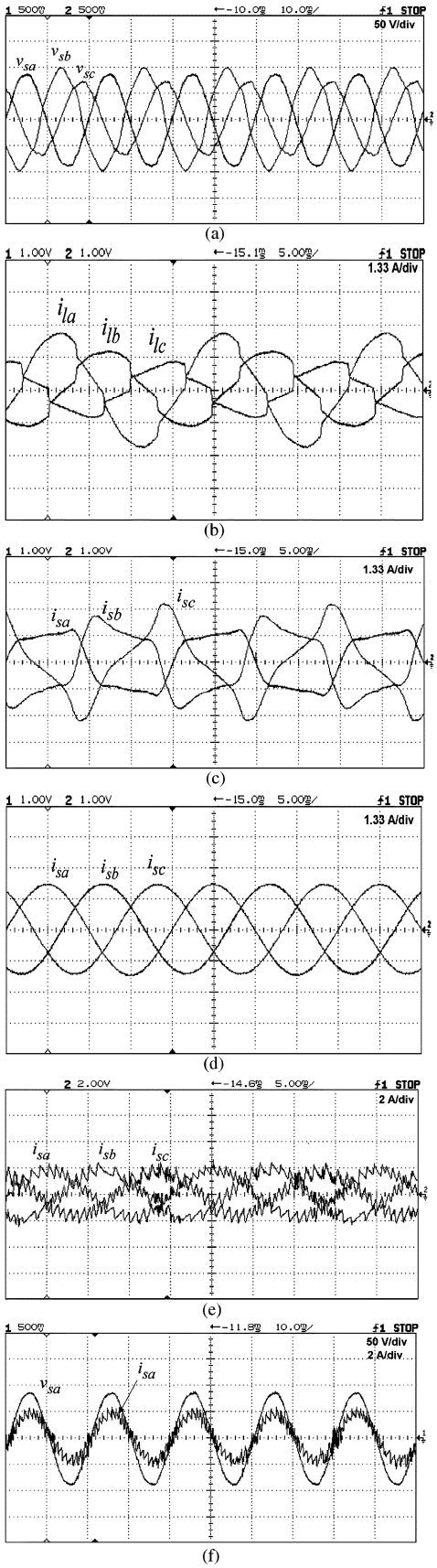

Fig. 11. (a) Unbalanced 3-phase supply voltages. (b) Load currents. (c) Compensated source currents with direct application of shunt algorithms. (d) Source currents with ideal compensator. (e) Source currents with real compensator. (f) Supply voltage and source current in phase-a.

source inverter is operated in hysteresis band current control mode to track the reference currents, the source currents after compensation are illustrated in Fig. 11(e). As evident, these currents form hysteresis envelope over the ideal source currents observed in Fig. 11(d). The unity phase relationship between phase-a supply voltage and phase-a source current is depicted in Fig. 11(f). These results are consistent with the results discussed in Section II.

VI. Conclusions

In this paper, it is shown that under unbalanced source voltages, the direct application of the shunt algorithms generally available in literature will result in erroneous compensation. Various modified algorithms namely equal current, equal power and equal impedance methods have been suggested. None of these methods provide completely balanced source currents. The proposed modified equal current algorithm alleviates this problem. This algorithm provides balanced and sinusoidal source currents irrespective of the magnitude and phase angle unbalance in source voltages. However, this scheme does not work when the source voltages are distorted. Under this condition, shunt algorithm with positive sequence extraction of source voltages is used for the generation of the reference compensator currents. The method provides an excellent performance of the compensator under unbalanced and the distorted voltages.

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