AIP | Applied Physics Letters

Work function tuning and improved gate dielectric reliability with multilayer graphene as a gate electrode for metal oxide semiconductor field effect device applications

Abhishek Misra, Mayur Waikar, Amit Gour, Hemen Kalita, Manali Khare, Mohammed Aslam, and Anil Kottantharayil

Citation: Applied Physics Letters **100**, 233506 (2012); doi: 10.1063/1.4726284
View online: http://dx.doi.org/10.1063/1.4726284
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/100/23?ver=pdfcov
Published by the AIP Publishing

Work function tuning and improved gate dielectric reliability with multilayer graphene as a gate electrode for metal oxide semiconductor field effect device applications

Abhishek Misra,[1,a)] Mayur Waikar,[1] Amit Gour,[1] Hemen Kalita,[2] Manali Khare,[1] Mohammed Aslam,[2] and Anil Kottantharayil[1,a)]
[1]*Department of Electrical Engineering and the Centre of Excellence in Nanoelectronics, Indian Institute of Technology Bombay, Mumbai, India*
[2]*Department of Physics, Indian Institute of Technology Bombay, Mumbai, India*

(Received 27 April 2012; accepted 22 May 2012; published online 6 June 2012)

Graphene with varying number of layers is explored as metal gate electrode in metal oxide semiconductor structure by inserting it between the dielectric (SiO_2) and contact metal (TiN) and results are compared with TiN gate electrode. We demonstrate an effective work function tuning of gate electrode upto 0.5 eV by varying the number of graphene layers. Inclusion of even 1-3 layers of graphene results in significantly improved dielectric reliability as measured by breakdown characteristics, charge to breakdown, and interface state density. These improvements are attributed to the impermeability of graphene for TiN and hence reduced metallic contamination in the dielectric. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4726284]

Metal gates are considered essential in advanced complementary metal oxide semiconductor (CMOS) technology for continued scaling.[1] However, the interfacial interactions of the metal gate with the underlying dielectric is a serious concern[2] as this could lead to fermi level pinning[3] and cause contamination in the thin gate dielectrics and thus degrade the device reliability.[4] Some of these concerns are addressed using a replacement gate process[5,6] which avoids high temperature processing after the metal gate deposition. However, the replacement gate process is complex and hence is not widely used in CMOS technology. Graphene (Gr), because of its two dimensional sheet like structure, extraordinary high conductivity, and high thermal stability, can be an interesting candidate as a gate material in MOS devices. For any material intended to be used as a gate electrode in MOS technology, knowledge of its work function (WF) is very essential. WF of graphene with different number of layers is studied by a number of techniques like Kelvin probe force microscopy (KPM),[7–10] photoelectron emission microscopy,[11] and by measuring the open circuit voltage in graphene based solar cells.[12] WF of graphene is also a subject matter of intense modeling efforts.[13,14] Theoretically, the doping of graphene by metals modeled by Giovannetti *et al.*[13] predicted that the WF of graphene would increase (decrease) when it is doped with metals with higher (lower) work function than that of graphene due to electron transfer for Fermi level alignment. However Pi *et al.*[15] experimentally demonstrated that the graphene would be n-doped when in contact with Pt, contradicting the predictions in Ref. 13. Further, graphene work function is known to increase with the dielectric constant of the dielectric on which it is deposited.[8,16]

Most of the experimental studies performed so far converge to a monotonous increase in the Gr WF as the number of layers increases and it saturates to some value for more than 4–6 layers. WF of Gr on SiC increases from 4.2 eV for single layer graphene (SLG) to 4.6 eV for more than 4 layers as measured by KPM method[11] while for Gr on Si, same trend of increasing WF from a value of about 4.35 eV for monolayer to 4.61 eV for more then 4 layers is reported.[12] WF of Gr on SiO_2 as measured by KPM method also increases from 4.57 eV for SLG to 4.69 eV for bilayer graphene (BLG).[10] Theoretical studies of Ziegler *et al.*[14] predicted that graphene WF depends on the carrier concentration and doping type for 1 to 3 layers of graphene and WF is insensitive to doping for thicker layers. It is clear that the WF of graphene for any application should be determined in the material environment in which it is being used.

Recently, Park *et al.*[17] proposed the use of monolayer graphene synthesized by CVD as the gate metal in charge trap memory devices. Since graphene is extremely thin, a metal for making contacts for measurements is required. Park *et al.* had deposited nickel on a small area on top of Gr for this purpose. They have compared the performance of such devices with devices containing TaN as gate metal. Significant improvement in the memory performance is demonstrated for graphene gated devices compared to TaN gated devices.[17] The performance improvement is attributed to the higher work function of the monolayer graphene on Al_2O_3 compared to the WF of TaN and reduced mechanical stress in the underlying gate dielectric.

In summary, even though Gr can be an interesting candidate for gate applications in MOS devices, no study of the WF of Gr as a function of the number of layers using MOS test structures is reported in available literature. In this report, we systematically study the electrical performance of multi layer graphene (MLG) gate electrodes with varying number of Gr sheets under the TiN contact metal for the MOS technology. Here, TiN is used as the contact layer as this material is widely used as interconnect metal diffusion barrier in state of the art CMOS technology. We demonstrate that the effective work function of gate electrode in a TiN/Gr/SiO_2 system can be tailored over a range of 0.5 eV by

[a)]Authors to whom correspondence should be addressed. Electronic addresses: mabhishek@ee.iitb.ac.in and anilkg@ee.iitb.ac.in.

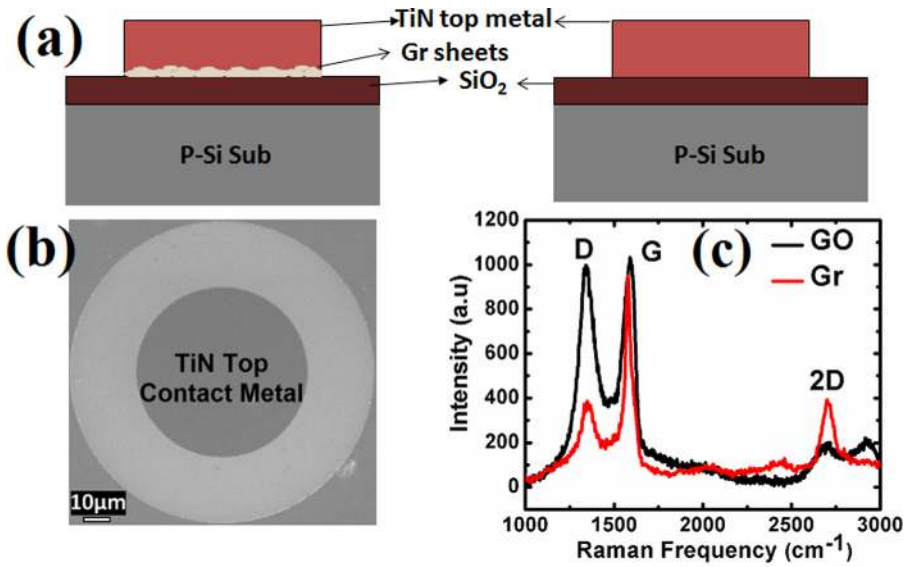

FIG. 1. (a) Schematic of the devices with and without Gr sheets sandwiched between TiN gate electrode and SiO_2 gate dielectric. (b) Top view of as fabricated MOS-capacitor. (c) Raman spectra of GO and graphene obtained after thermal reduction of GO.

using multilayer graphene with different number of layers. We also demonstrate improved reliability of the SiO_2 in TiN/Gr/SiO_2 system than in TiN/SiO_2 system and a conceptual model to explain this observation is proposed.

To evaluate multi layer graphene as a gate electrode material, MOS-capacitor structures with and without graphene are fabricated on P type Si substrate (resistivity of 1–5 Ω cm) with 7.6 nm (±0.2 nm) thermally grown SiO_2 as the gate dielectric. Schematic of the cross section and the top view SEM of as fabricated MOS capacitors are shown in Figs. 1(a) and 1(b), respectively. Thickness of the SiO_2 films is measured using a spectroscopic ellipsometer (Sentech, SE 800). After the growth of gate oxide, graphene oxide (GO) obtained by Hummer's method is deposited on gate dielectric by drop cast technique and it is thermally reduced to Gr at 500 °C in Ar ambient for 1 h. The same procedure of thermal reduction of GO into Gr at the device locations was demonstrated earlier.[18] Raman spectra of GO and thermally reduced graphene sheets are shown in Fig. 1(c). Thermal reduction results in an enhancement in the 2D band at ~2700 cm^{-1} and a suppression of the defect related D band at ~1350 cm^{-1}. Further, ratio of D band intensity to G band intensity decreases, from 0.97 for GO to 0.40 for reduced graphene. The G band is seen to shift towards lower wave number from 1590 cm^{-1} for GO to 1580 cm^{-1} for reduced graphene. These observations attest to the reduction of GO into graphene like character.[19,20] Further, adhesion of Gr with the underlying dielectric was also reported to improve after annealing.[16] Different ranges of Gr thicknesses are obtained by varying the number of drop casts i.e., one drop cast of liquid at some locations while multiple drop casts at other. To make the devices with varying number of Gr layers under the contact metal, extensive scanning electron microscopy (SEM) is performed in an electron beam lithography system (RAITH 150TWO) to identify the location of various thicknesses of graphene (very thin, moderate thin, and thick) on the gate dielectric and co-ordinates of these locations are stored for further top gate patterning. SEM and atomic force microscopy (AFM) (Vecco Digital Instruments, Nanoscope IV) images of very thin, moderate thin, and thick layer graphene sheets are shown in Figs. 2(a)–2(f). It is seen that the thinnest films obtained are not continuous and as the thickness increases, closed films of multi layer Gr are obtained. Figs. 2(g)–2(i) show the corresponding AFM sectional analysis of the height profile of Gr on SiO_2. Fig. 2(g) shows the sectional analysis for the thinnest films. The discrete topographical levels indicate different layers of graphene. The minimum height differences between discrete levels in the figure are in the range of 0.5 nm, which is consistent with literature data for Gr obtained by reduction of GO.[20] From the height profile of AFM images, thickness of very thin graphene sheets is about 0.5–1.5 nm, i.e., 1-3 layers (Fig. 2(g)), thickness of moderate thin graphene sheets is about 1.5–2.5 nm, i.e., 3–5 layers (Fig. 2(h)) while thickness of thick graphene sheets is more than 2.5 nm, i.e., more than 5 layers (Fig. 2(i)). In Figs. 2(g)–2(i), dashed lines show the low and high levels in the line scans. The spikes beyond the dashed lines observed at few sites correspond to the local variation in the Gr thickness or the number of Gr layers. However, the width of these spikes is small (~50 nm) compared to the overall gate dimensions of the MOS-capacitors and hence will not affect the characteristics of the capacitors significantly. TiN as top contact electrode is deposited by sputtering process (Applied Material ENDURA). PMMA is spin coated on the sample and circular patterns of TiN dots of 80 μm diameter are patterned at the already noted coordinates by electron beam lithography system (RAITH 150Two). This procedure affirms the presence of graphene sheets of different known thickness under the TiN contact metal. Finally, dry etching of the TiN is performed in Cl_2 + BCl_3 plasma and graphene sheets are etched by O_2 plasma in a reactive ion etching system (Applied Material Etch Centura). On the same wafer, a region without graphene sheets is also identified using the same SEM system for control devices (TiN/SiO_2/Si).

Both kinds of MOS-capacitors (with and without graphene) are electrically characterized using Agilent 4284 LCR meter and Agilent 4156C semiconductor parameter analyzer. Capacitance-voltage (C-V) and conductance-voltage (G-V) plots of these devices are shown in Figs. 3(a) and 3(b), respectively. As the number of Gr layers increases, C-V curves shift rightwards. This is due to the increasing

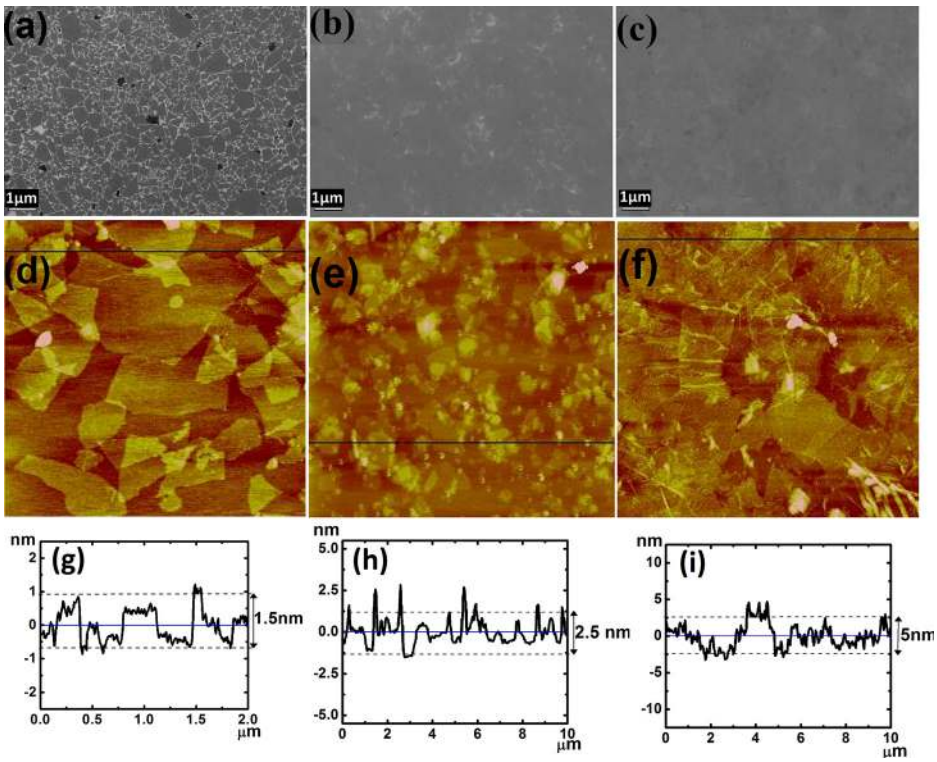

FIG. 2. (a)–(c) SEM images of different layers of Gr; (a) 1–3 layers of Gr sheets, (b) 3–5 layers of Gr sheets, (c) more than 5 layers of Gr sheets. (d)-(f) AFM images of Gr sheets corresponding to figure (a)–(c), respectively. (g)–(i) AFM sectional analysis showing the thickness of Gr sheets corresponding to (d–f), respectively. Note the vertical scales in the AFM sectional data. The discrete steps in (g) correspond to different layers of graphene.

WF of the graphene with increasing number of layers.[8–12] Variation of the flatband voltage with increasing number of Gr layers in TiN/Gr electrode is shown in Fig. 3(c). We calculate the work function for the gate electrode using the equation[21] $V_{FB} = \Phi_{ms} - Q_{OX}/C_{OX}$, where V_{FB} is the flatband voltage, Φ_{ms} is the WF difference between the gate electrode and the semiconductor substrate, Q_{ox} is the fixed oxide charge, and C_{OX} is the oxide capacitance. WF for TiN electrode as calculated from the given equation is 4.45 eV while for TiN/Gr stack, it has a value of 4.6 eV, 4.74 eV, and 4.91 eV for thin graphene, moderate thick graphene, and thick graphene, respectively. In these calculations, a substrate doping of 3E15 cm^{-3} is used (calculated from C_{min} value of high frequency C-V curve) and since all the MOS capacitors are made on same wafer under identical process conditions, it is assumed that the effect of fixed oxide charges on the flatband voltage is same for all devices.[21] The WF of TiN obtained in present study is within the range of

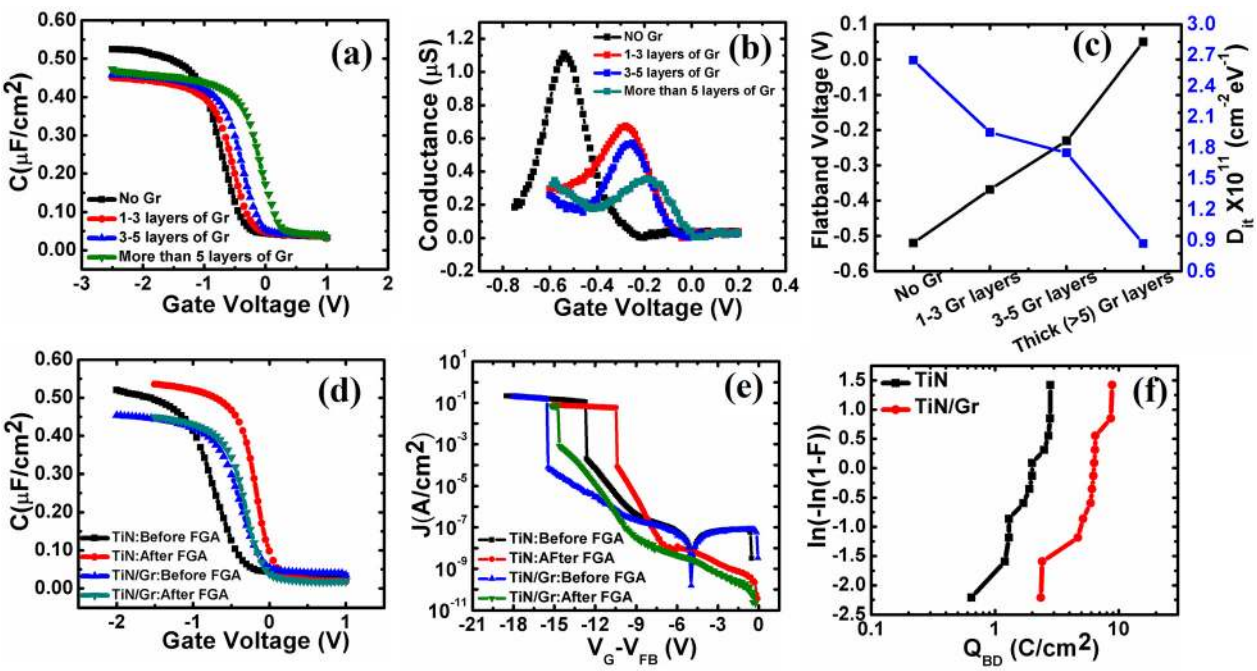

FIG. 3. (a) and (b) Comparison of C–V and G–V plots, respectively, for TiN gate electrode and TiN/Gr gate electrode devices with different numbers of graphene layers. (c) Flatband voltage and the interface state density with increasing number of graphene layers in TiN/Gr electrode devices. (d) and (e) C–V and J–V plots of TiN/SiO_2 and $TiN/Gr/SiO_2$ devices before and after FGA at 420 °C for 20 min with 3–5 layers Gr and (f) charge to breakdown behavior for only TiN and TIN/Gr gate electrode devices.

the WF values reported in the literature for PVD deposited TiN on SiO_2.[22] The values of Gr WF on SiO_2 reported in the literature vary between 4.45 eV and about 5 eV for SLG to MLG depending on the type of Gr, measurement technique and contact metal used.[7,10,14] The work function values, obtained in this work, for different number of Gr layers on SiO_2 are in close agreement with the WF values reported in the literature for few layer (4.57 eV for SLG, 4.69 eV for bi layer graphene)[10] and multilayer (4.93 eV to 4.95 eV for MLG) exfoliated graphene on SiO_2, all obtained by KPM method.[7] When Gr is deposited on the dielectric, strong hole doping from the underlying dielectric causes a significant increase in the WF of Gr compared to its value in the suspended state.[8,14] Moreover, higher the dielectric constant of the dielectric, more hole doping is expected.[16] In Ref. 17, work function of monolayer graphene is reported to be about 5.2 eV–5.3 eV on Al_2O_3 which has a higher dielectric constant than that of SiO_2. Since in the present study, WF of TiN is almost equal to the reported values of the WF of Gr, we do not expect any significant charge transfer between TiN and Gr. These results suggest that the role of TiN in a TiN/Gr stack is to provide contact whereas the Gr layers decide the WF. This may be an important technique for the WF tuning of the gate electrode in MOS devices provided that a methodology to deposit Gr films with control on the number of layers is developed.

Another observation in C-V plots is that the accumulation capacitance is lower for TiN/SiO_2 stack compared to the $TiN/Gr/SiO_2$, irrespective of the thickness of the Gr. Effective oxide thickness (EOT) calculated from the accumulation capacitance for TiN electrode is 6.6 nm while EOT for TiN/Gr electrode is 7.5 nm to 7.3 nm. The EOT of the gate dielectric for TiN electrode is about 1 nm less than the value obtained from ellipsometry while EOT for TiN/Gr electrodes is less by only about 0.1 to 0.3 nm. This indicates the consumption of the dielectric by some chemical reaction at the TiN/SiO_2 interface. Any chemical reaction at metal/dielectric interface is undesirable as it could lead to fermi level pinning[3] and causes contaminations in the thin gate dielectrics and thus degrade the device reliability.[4] Further, diffusion of metal in the underlying dielectric degrades the insulating behavior of the gate dielectric.[2,4] The reduction of EOT with metal gate electrode via chemical reaction at metal/dielectric interface is also reported in literature.[23] In our study, the chemical reaction at the metal/dielectric interface ceases to happen even when 1–3 layers of Gr are sandwiched between metal and the dielectric.

Inclusion of graphene between metal and dielectric also improves the interface quality as clearly seen in G-V plots shown in Fig. 3(b). Conductance peak in the G-V plot indicates the amount of interface states at the SiO_2/Si interface and the peak position occurs around the flatband voltage of the devices. With the increasing number of graphene layers in the device, G-V peak height reduces. The peak position also shifts towards right and this is in accordance with the increasing WF of the graphene with increasing number of layers. Interface states calculated as per the equation given in Ref. 24 are plotted in Fig. 3(c). Values of the interface states reduce from $2.7 \times 10^{11}\,cm^{-2}\,eV^{-1}$ for only-TiN electrode to a value of $8 \times 10^{10}\,cm^{-2}\,eV^{-1}$ for the devices with more than 5 layers of Gr under TiN. In the present study, TiN is deposited by sputtering process which invariably causes some damage to the SiO_2/Si interface. An improvement in the SiO_2/Si interface quality suggests that graphene, because of its superior mechanical properties, shields the SiO_2/Si interface from sputtering damage.

We have also investigated the robustness of the gate stacks to thermal anneal. C-V characteristics of the TiN/SiO_2 and $TiN/Gr/SiO_2$ before and after forming gas anneal (FGA) at 420 °C for 20 min are shown in Fig. 3(d). Improved slope of the C-V curves after FGA signifies the reduced interface state density.[21] The C-V curve of the TiN/SiO_2 has shifted to the right after FGA, indicating an increase in negative fixed charges in the oxide or an increase in the WF or both.[22] This is likely due to an increased interaction between TiN and SiO_2 at the temperature used for the FGA. However, the $TiN/Gr/SiO_2$ is seen to be robust against FGA, except for the (beneficial) improvement in interface state density.

Graphene gate electrode also results in much improved breakdown characteristics of the devices. Fig. 3(e) compares the current density versus gate voltage plots for TiN electrode and TiN/Gr electrode before and after FGA. TiN/Gr electrode devices have lower leakage compared to TiN electrode devices. This improvement in the breakdown characteristics of the devices is independent of the number of Gr layers in the TiN/Gr electrode. Average breakdown fields for TiN and TiN/Gr devices are 17 MV/cm and 20.5 MV/cm, respectively, before FGA, while after FGA, breakdown fields for TiN and TiN/Gr electrode devices are 16.1 MV/cm and 19.7 MV/cm, respectively. Further, charge to breakdown (Q_{BD}) is an important figure of merit for qualifying the dielectric reliability.[25] We performed Q_{BD} measurements on TiN and TiN/Gr electrode devices under identical constant current stress. Fig. 3(f) shows the Q_{BD} characteristics for both kinds of devices. Average value of Q_{BD} for $TiN/Gr/SiO_2$ devices is about $6\,C/cm^2$ while Q_{BD} value for TiN/SiO_2 devices is only $2\,C/cm^2$.

Based on the electrical data discussed above, we conclude that incorporation of Gr between contact metal and gate dielectric significantly improves the dielectric reliability. Park *et al.*[17] reported improved performance of charge trap flash memory using monolayer Gr as gate dielectric and attributed this to the relaxation of the stress on the dielectric stack when Gr is used. However, a reduction in EOT seen in our experiment cannot be explained by stress relaxation. A possible contributor to the improved dielectric reliability in the present study is the impenetrability of graphene by TiN, apart from the shielding of the dielectric from the sputtering damage. The impermeability of graphene for TiN can be explained by considering the area of the graphene hexagon and the size of TiN molecule. The distance between the opposite edges of Gr hexagon is about 2.46 Å (Ref. 26) this suggests that the maximum diameter of a sphere which can permeate through the Gr hexagon is about 2.46 Å. Ti-N has a bond length of about 1.57 Å (Ref. 27) and Ti and N have atomic diameters of 2.84 nm and 1.36 nm, respectively.[28] This implies that TiN, being larger than the Gr hexagon, would not permeate through Gr film as demonstrated in Fig. 4. As a result, even a single defect free Gr layer would prevent the metal diffusion into the dielectric and hence the

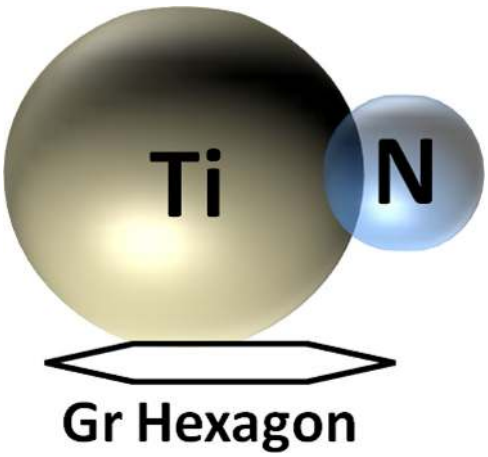

FIG. 4. TiN is larger than the Gr hexagon. As a consequence, Gr is impermeable to TiN (or for that matter any metallic compound that is larger than Gr).

metal/dielectric reaction would be suppressed. Possibility of diffusion of metals like Co, Ni, and Au in Gr is also ruled out in the literature.[29]

We have demonstrated that Gr can be a potential candidate for gate application in CMOS devices in combination with TiN contact metal. Incorporation of graphene between contact metal and gate dielectric not only results in the improved gate dielectric reliability by preventing any interaction between TiN and dielectric but also results in the WF of the gate electrode tuned over a range of 0.5 eV by varying the number of graphene layers. The gate stack with TiN/Gr electrode is more robust against thermal treatment compared to only-TiN electrode devices.

This work is carried out at the Centre of Excellence in Nanoelectronics (CEN) at IIT Bombay, which is supported by the Department of Information Technology of the Government of India. We acknowledge the IRCC-FIST (Physics) central SPM facility and the Sophisticated Analytical Instrument Facility at IIT Bombay for AFM and Raman measurements, respectively.

[1]International Technology Roadmap for Semiconductors, 2010 edition.
[2]T. Ushiki, K. Kawai, I. Ohshima, and T. Ohmi, IEEE Trans. Electron Devices **47**, 2201 (2000).
[3]H. Y. Yu, C. Ren, Y. C. Yeo, J. F. Kang, X. P. Wang, H. H. H. Ma, M. F. Li, D. S. H. Chan, and D.-L. Kwong, IEEE Electron Device Lett. **25**, 337 (2004).
[4]V. Misra, G. Lucovsky, and G. Parsons, MRS Bull. **27**, 212 (2002).
[5]A. Chatterjee, R. A. Chapman, K. Joyner, M. Otobe, S. Hattangady, M. Bevan, G. A. Brown, H. Yang, Q. He, D. Rogers, S. J. Fang, R. Kraft, A. L. P. Rotondaro, M. Terry, K. Brennan, S.-W. Aur, J. C. Hu, H.-L. Tsai, P. Jones, G. Wilk, M. Aoki, M. Rodder, and I.-C. Chen, Tech. Dig. - Int. Electron Devices Meet. **1998**, 98.
[6]C. Ren, H. Y. Yu, J. F. Kang, X. P. Wang, H. H. H. Ma, Y.-C. Yeo, D. S. H. Chan, M.-F. Li, and D. L. Kwong, IEEE Electron Device Lett. **25**, 580 (2004).
[7]N. J. Lee, J. W. Yoo, Y. J. Choi, C. J. Kang, and D. Y. Jeon, Appl. Phys. Lett. **95**, 222107 (2009).
[8]S. S. Datta, D. R. Strachan, E. J. Mele, and A. T. Charlie Johnson, Nano Lett. **9**, 7 (2009).
[9]T. Filleter, K. V. Emtsev, T. Seyller, and R. Bennewitz, Appl. Phys. Lett. **93**, 133117 (2008)
[10]Y. J. Yu, Y. Zhao, S. Ryu, L. E. Brus, K. S. Kim, and P. Kim, Nano Lett. **9**, 3430 (2009).
[11]H. Hibino, H. Kageshima, M. Kotsugi, F. Maeda, F.-Z. Guo, and Y. Watanabe, Phys. Rev. B **79**, 125437 (2009).
[12]K. Ihm, J. Tim, K. J. Lee, J. W. Kwon, T. H. Kang, S. Chung, S. Bae, J. H. Kim, B. H. Hong, and G. Y. Yeom, Appl. Phys. Lett. **97**, 032113 (2010).
[13]G. Giovannetti, P. A. Khomyakov, G. Brocks, V. M. Karpan, J. van den Brink, and P. J. Kelly, Phys. Rev. Lett. **101**, 026803 (2008).
[14]D. Ziegler, P. Gava, J. G. uttinger, F. Molitor, L. Wirtz, M. Lazzeri, A. M. Saitta, A. Stemmer, F. Mauri, and C. Stampfer, Phys. Rev. B **83**, 235434 (2011).
[15]K. Pi, K. M. McCreary, W. Bao, W. Han, Y. F. Chiang, Y. Li, S.-W. Tsai, C. N. Lau, and R. K. Kawakami, Phys. Rev. B **80**, 075406 (2009).
[16]S. M. Song and B. J. Cho, Nanotechnology. **21**, 335706 (2010).
[17]J. K. Park, S. M. Song, J. H. Mun, and B. Jin Cho, Nano Lett. **11**, 5383 (2011).
[18]X. Wang, L. Zhi, and K. Mullen, Nano Lett. **8**, 323 (2008).
[19]L. Liu, S. Ryu, M. R. Tomasik, E. Stolyarova, N. Jung, M. S. Hybertsen, M. L. Teigerwald, L. E. Brus, and G. W. Flynn, Nano Lett. **8**, 1965 (2008).
[20]M. J. Allen, V. C. Tung, and R. B. Kaner, Chem. Rev. **110**, 132 (2010).
[21]E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, New York, 1982), p. 468.
[22]J. Westlinder, G. Sjoblom, and J. Olsson, Microelectron. Eng. **75**, 389 (2004).
[23]G. S. Lujan, T. Schram, L. Pantisano, J. C. Hooker, S. Kubicek, E. Rohr, J. Schuhmacher, O. Kilpelä, H. Sprey, S. De Gendt, and K. De Meyer, in *Proceedings of the European Solid State Devices Research Conference* (2002), p. 583.
[24]W. A. Hill, C. C. Coleman, Solid-State Electron **23**, 987 (1980).
[25]E. Rosenbaum, J. C. King, and C. Hu, IEEE Trans. Electron Devices **43**, 70 (1996).
[26]F. Schwierz, Nat. Nanotechnol. **5**, 487 (2010).
[27]Y. C. Bae, H. Osanai, K. Ohono, M. Sluiter, and Y. Kawazoe, Mater Trans. **43**, 482 (2002).
[28]C. Ma, S. Ishihara, H. Soejima, N. Nishiyama, and A. Inoue, Mater. Trans. **45**, 1802 (2004).
[29]S. Entani, S. Sakai, Y. Matsumoto, H. Naramoto, T. Hao, and Y. Maeda, J. Phys. Chem. C. **114**, 20042 (2010).