Tutorial T3B

System Aspects of Analog to Digital Converter Designs

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Abstract

Section 1 - Introduction:
In this section the principles of operation of data-converters, the different architectures, and the important specification parameters are presented. We begin by discussing the fundamental processes of analog-digital conversion: quantization, sampling, resolution. The various figures-of-merit of an ADC such as Integral Non-Linearity (INL), Differential Non-Linearity (DNL) and Signal-Noise Ratio (SNR) are then presented. In the second part of this section, a classification of well-known A/D converter architectures is presented. The advantages and disadvantages of each of these architectures, their respective resolution-speed-power consumption ranges, and the applications in which they find use are discussed.

Section 2 - System aspects: ADCs find uses in a myriad of applications such as Communication Systems, Audio/Video Applications and Control Systems. The performance required from the ADC is different in each case depends on the signal characteristics of the system. The ADC's resolution is determined by the SNR required by the system, the RMS and Peak-to-Average Ratio of the signals, and the interferers present in the system. The sampling frequency is determined by the signal bandwidth as well as the filtering requirements. As an example, we consider a wireless system to illustrate how the ADC specifications are derived. By optimizing the analog functions of the system, we can significantly reduce the cost and the power dissipation of the system. In the last part of this section, we demonstrate this by comparing the cost/design complexity of a given wireless system with three different ADC performances.

Section 3 – Recent advances in ADCs: Recent innovations have resulted in ADC implementations with higher performance (resolution and speed) and reduced power dissipation. This section summarizes some of the key technical innovations in the design of pipeline, discrete-time and continuous-time sigma-delta ADCs. The last part of the tutorial presents a case study of a wireless system that has been optimized to exploit the improved ADC performance.

The target audience for this tutorial is analog and system designers who are involved in the design of System-on-a-Chip. Given the flexibility offered by the digital process, the performance and the power of the SoC can be improved by moving the ADC up the signal chain. Most of the signal processing can be done in the digital obviating the need for complex analog functions. This tutorial discusses the trade offs involved in designing this optimum system solution and the design of high performance ADC.

Presenter Biography

Dr Shanthi Pavan is on the faculty of the Indian Institute of Technology-Madras, where he teaches, conducts research and consults for several companies in the areas of analog circuit design and signal processing. Prior to this Dr Shanthi Pavan worked at Texas Instruments and Big Bear networks where he worked on high speed ADCs, continuous-time filters and adaptive filters for ultra-high speed data communication.

Prakash Easwaran is VP-Systems in Cosmic Circuits. Prior to this, he worked in the mixed signal Products group at Texas Instruments India where he focused on the design of analog filters, PLLs, ADCs and analog systems for communications.

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