Simultaneous optical digital half-subtraction and -addition using SOAs and a PPLN waveguide

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Abstract: We demonstrate an optical half-subtracter and half-adder module that performs simultaneous bit-wise subtraction and addition of two 5 Gbit/s RZ data streams. We generate Borrow (/X•Y) and Difference/Sum (X⊕Y, or XOR) outputs using cross-gain modulation (XGM) in two parallel SOAs. Taking advantage of the gain saturation inherent to SOAs, we generate two signals, /X•Y, and X•/Y, and combine them using a passive optical coupler to generate the XOR Difference/Sum output. We use difference-frequency-generation-based λ-conversion in a PPLN waveguide to generate the Carry (X•Y) output. The PPLN waveguide allows bit-synchronous wavelength shifting, is wide-bandwidth, and offers no intrinsic chirp. Our module uses three active elements to perform simultaneous half-subtraction and addition, and carries a maximum power penalty of 1.0 dB.

OCIS codes: 060.2360 Fiber optics subsystems; 070.4340 Nonlinear optical signal processing

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1. Introduction

There has been renewed interest in the possibility of all-optical networks, where signals are transmitted, routed, and processed optically at high-speed line rates [1]. However, this vision might require many functions not currently realized in the optical domain, including optical address recognition, packet forwarding, routing-loop control/TTL decrementing, optical encoding/decoding of data, and packet checksum calculation [2-4]. It may also require signal processing devices, including optical digital logic gates, counters, shift registers, and half- and full-adders and subtracters for data encryption, key checking, or processing of packet headers. For this reason, there is value in demonstrating optical digital logic functions (e.g., AND/OR/XOR/XNOR) [5] and signal-processing functions (e.g., shift registers, subtracters, adders, (de-)multiplexers, and counters).

There have been recent demonstrations of some of these essential functions in the optical domain, including optical half-addition [6-7] and an optical shift register [8]. To our knowledge, however, there has yet to be a demonstration of an optical half-subtracter, nor a module that can perform simultaneous half-subtraction and -addition. Applications of an optical half-subtracter module include decrementing the time-to-live (TTL) packet header field, routing-loop control, dual-direction binary counters, encryption and decryption of data, packet checksum, and arithmetic-logic units (ALUs) [4, 9].

In this paper, we demonstrate simultaneous bit-wise half-subtraction and half-addition of two independent 5 Gbit/s input data streams. We generate "Borrow" (/X•Y, where /X represents the inverse of X, or 'X-bar') and "Difference/Sum" (X⊕Y, or XOR) outputs using cross-gain modulation (XGM) in two parallel semiconductor optical amplifiers (SOAs). Taking advantage of the gain saturation inherent in SOAs, we generate two signals, /X•Y, and X•/Y, and combine them using an optical coupler to generate the XOR "Difference/Sum". Since the SOAs generate /X•Y and X•/Y, we can tap off the /X•Y signal to use as the "Borrow" output, making the Borrow output "free" as a side-effect of the generation of "Difference/Sum". We use difference-frequency-generation (DFG) λ-conversion in a periodically-poled lithium niobate (PPLN) waveguide to generate the "Carry" (X•Y) output. The PPLN waveguide allows bit-synchronous wavelength shifting, is wide-bandwidth, and produces no intrinsic chirp. Our module uses only three active elements to perform both half-subtraction and addition, and carries a power penalty of ~1.0 dB.

2. Network architecture

The development of optical logic and signal processing may require a fundamental shift in architecture as one moves from electronics to optics. It may not be enough to simply "replace every electronic gate with an optical one" – some functions that may be trivial to construct using electronic elements may be difficult in optics, while the unique features inherent in optics (including nonlinearities and phase) may make optical implementations more realistic.

A key example is the comparison of the electronic and optical ALUs. In conventional electronics, addition is the default operation. In most cases, subtraction is done in an ALU by taking the "two's complement" of the subtrahend (B, in the equation "A-B=C") and adding A and B together. One reason is that it has been easier to construct adders than subtracters in conventional electronics; almost all electronic ALUs are build around the adder as a fundamental building block. However, this may not be true for optical systems, where a half-subtracter implementation may be more straightforward than that of a half-adder. Thus, it is not only enough to "build an electronic ALU with optics" but rather to consider the possibility of completely new architectures for optical networks – to do this, not only are examples of currently-used electronic functions required, but examples of optical implementation of functions often ignored in electronics may be useful in developing such new architectures.

3. Logic implementation

A digital gate-level conceptual diagram for a half-subtracter that implements the function 'X-Y' is shown on the left in Fig. 1(a). There are two digital inputs, 'X' and 'Y', and two

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outputs, “Difference”, and “Borrow”. The “Difference” output exists only when either ‘X’ or ‘Y’ exist (equals logic ‘1’), but not both (if both inputs to the subtracter equal one, 1 – 1 = 0). Thus, the output logical relationship for “Difference” is ‘X⊕Y’, commonly known as the exclusive OR (XOR), or parity, function. The XOR function, while not difficult to implement directly in electronics, has been found difficult to implement directly in the optical domain (although there have been some recent demonstrations [10]). However, this problem can be solved by breaking the XOR function down into the logical primitives of AND and OR, leading to the function ‘X•/Y + /X•Y’, and thus can be implemented using two AND gates with inverters (‘bubbles’) at the input, the outputs of which are followed by an OR gate. The “Borrow” signal exists only when it is necessary to subtract from a nonexistent signal (i.e. 0 – 1 = 1, plus a ‘Borrow’), and thus is represented by the logical function ‘/X•Y’. In the original conceptual diagram in Fig. 1(a), this required an additional gate. However, when implementing the “Difference” signal using AND/OR gates, the “Borrow” signal of ‘/X•Y’ is generated as an intermediate step toward “Difference”, and can be tapped off, generating the “Borrow” signal “for free” as a byproduct of generating “Difference”.

A gate-level implementation of a half-adder that implements the function ‘X+Y’ is shown in Fig. 1(b). There are two inputs, ‘X’ and ‘Y’, and two outputs, “Sum”, and “Carry”. The “Sum” output exists when one of the digital inputs, but not both, carries a value of logic ‘1’ (0 + 1 or 1 + 0 = 1). This is an XOR relationship, identical to that which is required to generate the “Difference” signal in the half-subtracter. Thus, it is not necessary, in this simultaneous half-subtracter/adder implementation, to include a separate set of gates for “Sum” – it also comes “free” as a result of generating “Difference” in the subtracter. The “Carry” output exists only when both the ‘X’ and ‘Y’ inputs are logic ‘1’ (i.e. 1 + 1 = 0, plus a ‘Carry’). This is the logical function ‘X•Y’, or AND, and can be represented by a single AND gate.

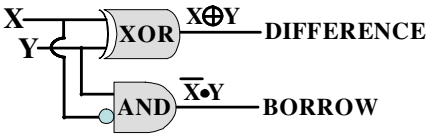
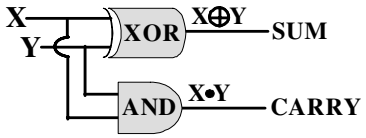


Fig. 1(a). Gate-level concept of half-subtracter.

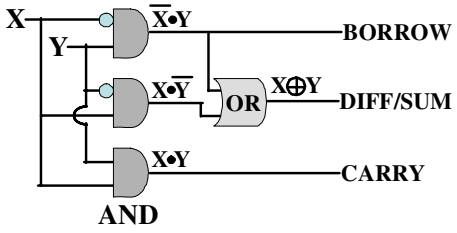


(b). Gate-level concept of half-adder.

A truth table showing the inputs and outputs for the half-subtracter and adder is shown in Fig. 2(a). Note the shaded area of the table, showing the similarity between the half-subtracter “Difference” output and the half-adder “Sum” output. Taking advantage of these similarities to create a single “master” gate-level implementation for the combined half-subtracter and half-adder, we obtain the construction shown in Fig. 2(b). The final implementation requires six gates – three AND, one OR, and two inverters.

Input data bits		Subtracter (X-Y)		Adder (X+Y)	
X	Y	Borrow	Diff.	Sum	Carry
0	0	0	0	0	0
0	1	1	1	1	0
1	0	0	1	1	0
1	1	0	0	0	1

Fig. 2(a). Truth table for half-subtracter and half-adder. Difference (subtracter) and Sum (adder) are identical.



(b). Gate-level diagram of combined half-subtracter/ adder using 6 gates (three AND, one OR, two inverters.

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4. Optical implementation

The optical half-subtracter/adder, as illustrated in Fig. 3, requires only three nonlinear optical elements, in contrast six electronic gates are usually required. The two blocks generate: (1) the Difference/Sum and Borrow outputs, and (2) the Carry output.

The upper block of the half-subtracter/adder is the XOR that will generate both the "Borrow" and the "Difference/Sum" outputs. The keys to this block are the two SOAs that generate outputs via XGM. In the XGM process, one high-power pump signal saturates the SOA gain, resulting in little residual gain available for any other probe signals. We consider the case of two synchronized co-propagating data streams 'X' and 'Y' located at λ_X and λ_Y, respectively. If 'X' is used as a pump, is at a significantly higher average power than 'Y', and an 'X' data bit is equal to '1' then the SOA gain is almost completely saturated. Therefore, a 'Y' data bit of any input value ('0' or '1') is suppressed, resulting in an output of a '0' [11]. Only when a 'Y' data bit is equal to '1' and the coinciding 'X' bit is '0' will any output be seen on λ_Y. This corresponds to a logical function of '/X•Y' on λ_Y. This output on λ_Y .

To generate the "Borrow" ('/X•Y'), input 'X' is used as the high-power pump signal and input 'Y' is the lower-power probe signal. In the second SOA in the upper block, 'Y' is used as the high-power pump signal and 'X' is the lower-power probe signal, thereby generating 'X•/Y'. A single 50:50 coupler is used as an OR gate, combining the two SOA outputs and generating the logic function 'X•/Y + /X•Y', or XOR – the required Difference/Sum output.

The lower block of the half-subtracter/adder enables the "Carry" for the half-adder; if half-adder functionality is not needed, this can be omitted. This block generates the 'X•Y' "Carry" signal using different frequency generation (DFG) in a PPLN waveguide. Using a cascaded $\chi(2):\chi(2)$ process, the PPLN waveguide acts as a wavelength conversion device that maps an input signal to a mirror-image wavelength with respect to a pump wavelength ($\lambda_C \approx 2*\lambda_X - \lambda_Y$) [12]. The λ-shifting process in the PPLN can be controlled on the order of a bit duration; by modulating the PPLN waveguide pump signal, a logic '1' bit on the input signal wavelength(s) is λ-shifted only when the pump signal is logic '1'. Thus, the output wavelength (λ_C) carries data that is the logical AND of the input signal and modulated pump. Additional advantages of PPLN DFG over SOA four-wave-mixing include its wide operational bandwidth (~50 nm), lack of intrinsic chirp, and negligible added noise.

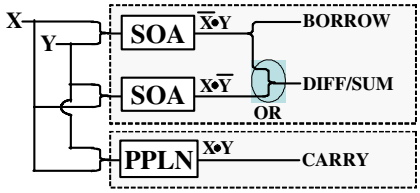

Fig. 3. Optical implementation of the half-subtracter/adder. This module uses three optical elements – two SOAs and one PPLN. The OR function is provided via an optical coupler. The upper block is all that is required for half-subtracter functionality, the lower block is required to include half-adder functionality.

5. Experimental setup

Figure 4 shows the experimental setup for the optical half-subtracter/adder, divided into the two blocks described above. The two data streams 'X' and 'Y' are generated by externally modulating two lasers at 1548.0 nm (λ_X) and 1550.1 nm (λ_Y) with 5 Gbit/s RZ pseudorandom data sequences up to 2^{11}-1; we stopped at 2^{11}-1 due to programming the pattern generator.

The 'X' and 'Y' inputs are both amplified to 18 dBm and combined using a 10:90 coupler. Coupler output port #1 uses the 'X' data signal (16.5 dBm output) as the high-power pump, and the 'Y' data signal (8 dBm) as the lower-power probe signal. Coupler output port #2 has the power levels reversed ('Y' at 16.5 dBm, 'X' at 8 dBm), and the 'Y' data signal acts as the pump signal while 'X' is the probe. The two coupler outputs are input to the two SOAs, both

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biased at 185 mA. 1546.0 nm CW assist light (shown in the figure) at 9 dBm is also coupled into each SOA along with the data signals. This input increases the efficiency of the XGM process by biasing the total average power closer to the saturation point [13].

The outputs of the two SOAs are filtered to isolate the low-power probe signal wavelength that carries the logical result desired and remove residual reflection in the SOA cavities. For SOA #1, the output signal on λ_Y carries '/X•Y'. For SOA #2, the output signal on λ_X carries 'X•/Y'. The output of SOA #1 is then split into two branches using a 50:50 coupler. One output branch of this coupler represents the '/X•Y' "Borrow" output for the half-subtracter. The other output branch is combined with an attenuated SOA #2 output to create the combined final output of '/X•Y + X•/Y', which is the "Difference" (XOR) of the half-subtracter. Should half-adder functionality also be desired, this output also represents the "Sum". The lower block of the module uses a single PPLN waveguide and is used to generate the "Carry". Input data signal 'Y' is used as the PPLN pump. Input signal 'X', at 1548 nm, is used as the probe signal, and the converted output signal is at a wavelength "mirrored" around the pump (~1552.2 nm). Input signals 'X' and 'Y' are amplified, combined using a 50:50 coupler, and injected into a polarizer, followed by the PPLN waveguide.

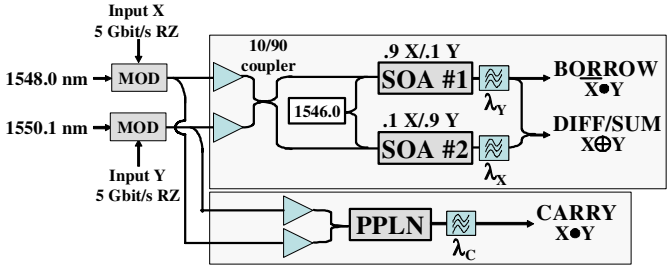

Fig. 4. Experimental setup for the half-subtracter/adder.

Figure 5 shows the PPLN output spectrum, including the 'Y' pump signal, 'X' probe signal, and -15 dBm converted output λ_{CARRY}. The conversion efficiency for a ~6 dBm input signal on λ_X is -21 dB. The output signal on λ_{CARRY}= 1552.2 nm is isolated via filtering, then amplified. This signal carries the logical function 'X•Y', which is the AND of the two data inputs, and is the "Carry" output for the half-adder portion of this module.

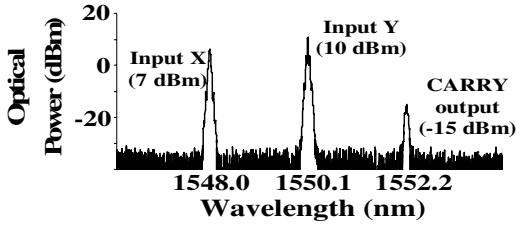

Fig. 5. Output optical spectrum of the PPLN. Conversion efficiency for 6 dBm input at 1548 nm is -21 dB.

6. Results and discussion

Representative bits from the inputs 'X' and 'Y' are shown in Figs. 6(a) and 6(b), respectively. The "Borrow" output of SOA #1 ('/X•Y') is shown in Fig. 6(c); an output pulse is present only when 'Y' is logic '1' and 'X' is logic '0'. The second output of the module, the "Difference/Sum" output, which is the combination of the outputs of SOA #1 and SOA #2, representing '/X•Y + X•/Y', is shown in Fig. 6(d); an output pulse is present when 'Y' is logic '1' or 'X' is logic '1', but not both. The 'X•Y' "Carry" output of the PPLN waveguide is shown in Fig. 6(e); an output pulse is present only when both 'X' and 'Y' are logic '1'.

The bit-error-rates for the half-subtracter/adder module are shown in Fig. 7. The "Carry" output shows a ~0.7 dB penalty when compared to the back-to-back case at 10^{-9}. The

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"Borrow" and "Difference/Sum" outputs show slightly higher penalties, with the SOA #1 "Borrow" output showing a ~0.8-dB penalty and the combined SOA #1 & #2 "Difference/Sum" output showing a ~1.0-dB penalty. Potentially, the "Carry" penalty could be reduced by using a PPLN waveguide with higher efficiency, and the "Borrow" and "Difference/Sum" penalties could be reduced by using SOAs that have lower noise, are more closely matched, and have a higher XGM efficiency. We observed little pattern dependence for our module for RZ data sequences from 2^7-1 to 2^{11}-1. The use of the NRZ might have more pattern dependence resulting from the XGM process.

A potential limitation is that the "Difference/Sum" output is carried on two wavelengths, as it is the combination of '/X•Y' output of SOA #1, which is carried on λ_Y, and 'X•/Y' output of SOA #2, which is carried on λ_X. For some applications, this may not be significant. However, in cases where data must be re-integrated into the optical data stream, it may be necessary to use an additional wavelength converter after SOA #2 prior to combining the two SOA outputs to ensure that all "Difference/Sum" pulses exist on the same output wavelength.

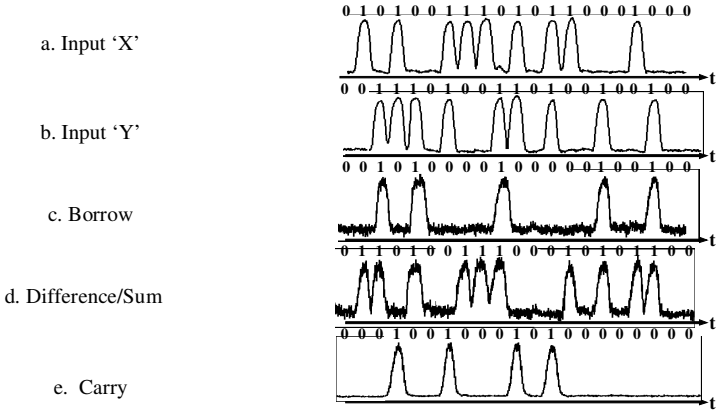

Fig. 6. (a). Input 'X' to the half-subtracter/adder module. (b) Input 'Y' to the half-subtracter/adder modules. (c) "Borrow" output of the half-subtracter. A pulse is present only if input 'Y' is logic '1' while input 'X' is logic '0'. (d) "Difference/Sum" output of the half-subtracter/adder. A pulse is present if input 'Y' is logic '1' or input 'X' is logic '1', but not both. (e) "Carry" output of the half-adder. A pulse exists only if both inputs 'X' & 'Y' are '1'.

We note that the upper block of the system setup (generating the "Borrow" and "Difference/Sum" outputs) is all that is required to create a half-subtracter, using two SOAs, as the "Borrow" signal is generated "free" as part of generating the "Difference/Sum". The additional PPLN waveguide is required only to generate the "Carry" for half-adder functionality (as the "Sum" also comes "free" as part of generating the "Difference" output). As the half-adder requires additional optical devices (either the PPLN or another SOA for four-wave-mixing) and the half-subtracter components (SOAs) are readily integrable optical components, it may be easier, in a future optical network, to use subtraction as a 'default' operation rather than the addition commonly used in electronic systems.

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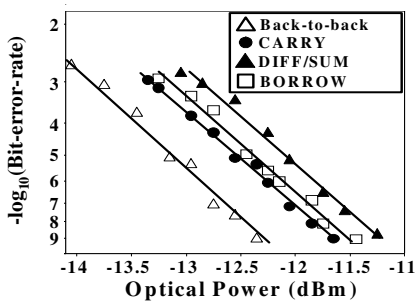

Fig. 7. BER for the half-subtracter/adder. The maximum penalty is ~1 dB.

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