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SIMULATION OF BI-DIRECTIONAL DC-DC CONVERTER USING FPGA

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Abstract

The basic idea of proposed system is to utilize the renewable resources by digital PWM control of Bi-directional DC – DC converter. Usually PWM pulse is being generated through a digital system such as microcontroller or Digital signal controller. In stand – alone application these controllers increases the cost but XILINX FPGA based PWM generation reduces the cost. XILINX FPGA is programmable device developed by XILINX which is being considered as an efficient device for rapid prototyping and also to perform concurrent operations. In this paper two PWM signals was generated to control the switch duty cycles in Bi-directional DC-DC Converter. In addition to that different modes of operation of the proposed circuit are verified by MATLAB / SIMULINK.

Peer-review under responsibility of the Organizing Committee of ICCCV 2016

Keywords: Bi-directional dc-dc converter, pulse width modulation; Field programmable gate array, XILINX, duty cycle.

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1. Introduction

.Interest in utility interactive photovoltaic inverter systems has increased over the past decade and numerous central-station photovoltaic systems have been installed. It is anticipated that as PV system cost decreases, the residential systems will be installed in increased number. The power converter (i.e) the DC – DC converter performs three functions: implementation of MPPT algorithm, Buck Converter & Battery Charger and Boost Converter.This paper focuses on Pulse Width Modulation (PWM) control of DC – DC converter output voltage depends on the Duty

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Cycle. Xilinx web pack software 9.2i used to generate PWM pattern by means of both schematic diagarams and VHDL programs. Xilinix FPGA's are standard integrated circuits that can be programmed by a user to perform a variety of complex logic functions. The high level of integration available with these devices (currently upto 500,000 gates) means that they can be used to implement complex electronic systems. Furthermore, there are many advantages due to the rapid design process and reprogrammable functions. Xilinx FPGA enables to produce prototype logic designs right in a short period. It is possible to create, implement and verify a new design. This is a sharp contrast to conventional gate array design processes, which can take months to produce working silicon. The final design is converted in configuration data file and loaded into SPRTAN – 3E board.

2. PROGRAMMABLE LOGIC DEVICES (PLD)

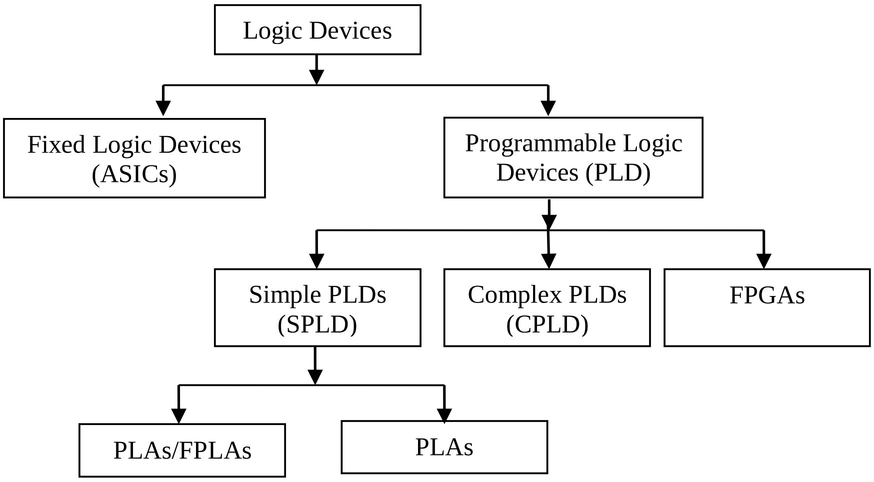


Fig:2 Programmable logic devices

2.*1 FIELD PROGRAMMABLE GATE ARRAYS (FPGAS)*

Field programmable gate arrays (FPGAs) are so-called because they are structured very much like the now-obsolete "Gate Array" form of Application Specific Integrated Circuit(ASIC). Inside the ring of I/O blocks lies a rectangular array of logic blocks and connecting logic blocks to logic blocks and I/O blocks to Logic Blocks is the programmable interconnect wiring.

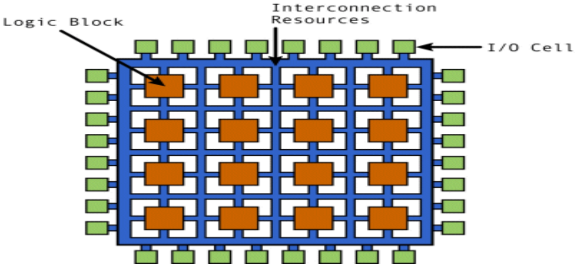


Figure 2.1 FPGA Architecture

2.2 ARCHITECTURE OF FPGA

The FPGA architecture consists of configurable logic blocks, configurable I/O blocks and programmable interconnect. Also, there will be clock circuitry for driving the clock signals to each logic block. Additional logic resources such as ALUs, memory and decoders may also be available. The three basic types of programmable elements for an FPGA are static RAM, anti-fuses and Flash EPOM.

2.3 CONFIGURABLE LOGIC BLOCKS (CLBS)

These blocks contain the logic for the FPGA. In the large grain architecture used by all FPGA vendors today, these CLBs contain enough logic to create a small state machine as illustrated in figure 2.4. The block contains RAM for creating arbitrary combinational logic functions also known as lookup tables(LUTs)..

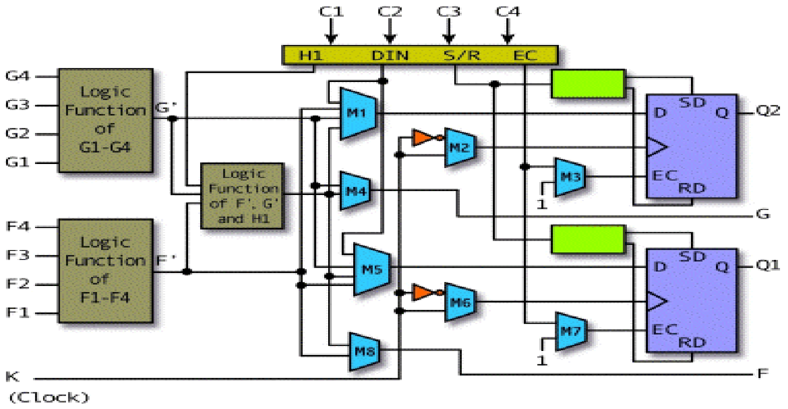


Figure 2.3Configurable Logic Blocks – Xilinx FPGA

The logic blocks within an FPGA can be as small and simple as the macro-cells in a PLD (called fine-grained architecture) or larger and more complex (coarse grained architecture). However, they are never as large as an entire PLD, as the logic blocks of a CPLD. But the logic blocks in an FPGA are generally nothing more than a couple of logic gates or a look-up table and a flip-flop.

3.BIDIRECTIONAL DC-DC CONVERTER

3.1 IMPORTANCE OF DC-DC CONVERTERS FOR PV APPLICATIONS

The choice of dc-dc converter must take into account the different aspects deriving from the need to supply the load with the greatest efficiency, minimizing volume, weight and cost. From the possibility of implementing control with good dynamic performance and from the reduction of filtering costs, which govern the choice of switching frequency range A variety of circuit technologies for switching power supplies are available.The most suitable switching frequencies and switching power devices are found for the different topologies and applications. The findings provide pointers to the optimum solutions in the case where optimization of efficiency and/or minimization of weight and space occupied by the dc-dc converter are the key points of issue.

3.2 PROPOSED CIRCUIT TOPOLOGY OF BIDIRECTIONAL DC-DC CONVERTER

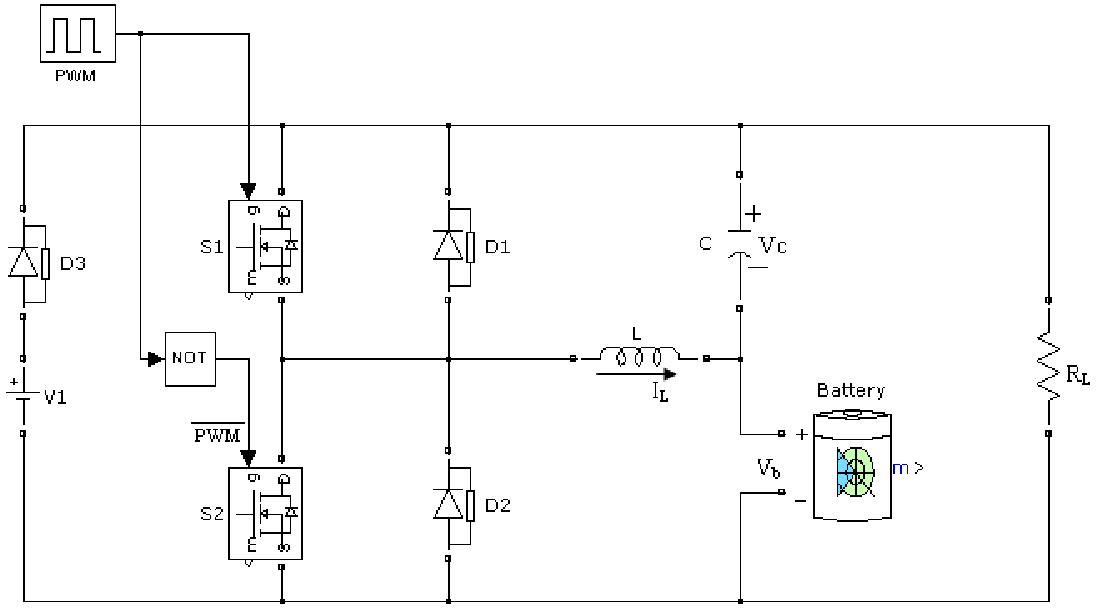


Fig 3.2 Bi-directional DC – DC Converter

If the supply voltage is not enough to supply the load, the power system operates as a boost converter, transferring energy from the battery to the load. In this case, while the switch S2 is turned ON, the inductor L stores energy from the battery as shown in Figure 3.4 & 3.5 When the switch S2 is turned OFF, the energy stroed in the inductor is transferred to the Load. Figure 3.6 shows the command signal of the power switches S1(VCS1) and S2(VCS2) and the inductor current waveform (IL) in the buck and boost operations.

4. FPGA BASED PWM GENERATION

4.1 GENERATION OF DUTY CYCLE

The duty cycle k can be generated by comparing a dc reference signal V_r, with a saw tooth carrier signal V_{cr}. This is shown in fig---, where V_r is the peak value of V_r and vcr is the peak value of V_{cr}, the reference signal.Where M is called the modulation index. By varying the carrier signal vcr from 0 to vcr, the duty cycle k can be varied from 0 to 1.

4.1. ALGORITHM TO GENERATED THE GATING SIGNAL IS AS FOLLOWS

1. Generate a saw tooth waveform of period T as the reference signal V_r and a dc carrier signal V_{cr}.
2. Compare these signals by a comparator to generate the difference $V_c - V_{cr}$ and then a hard limiter to obtain a square – wave gate pulse of width kT, which must be applied to the switching device through an isolating circuit. Any variation to V_{cr} varies linearly with the duty cycle k

5.PWM SIGNAL GENERATION AND SIMULATION RESULT

5.1 SAMPLE RATE CALCULATION

Xillinx Spartan – 3E kit clock frequency is 50MHz. So, Time is T=1/FT=1/50MHz=0.02µs.This nanosecond time is not measurable. So, clock frequency will be divided to our requirements.

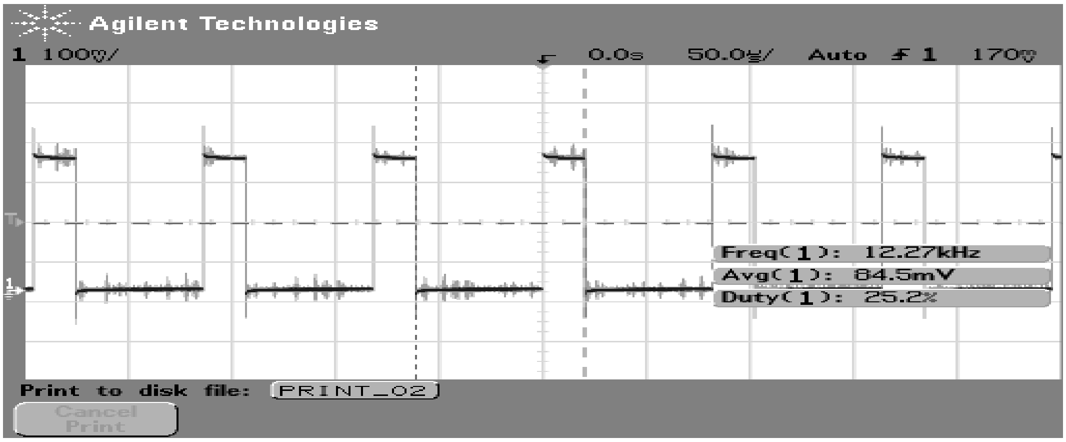
Design Frequency=50 KHz and Max. Count is FFF. This frequency and maximum count will be fixed and sampling time was varied.

Case(i) Sample rate=Design Frequency / Max. Count
= 50KHz/ 4096
=12.2 HZ.

Case(ii) Sample rate=6.25MHz/4096
= 1.525KHz.

5.2 PWM OUTPUT OBSERVER ON A DSO

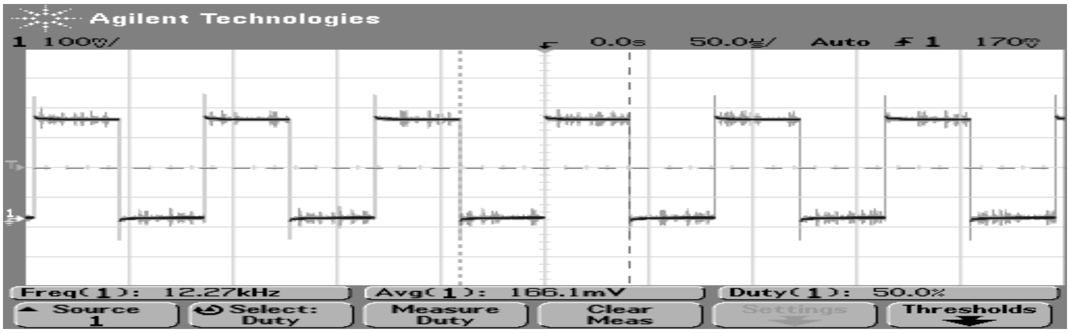
5.2.1 DUTY CYCLE 25%



Freq(1): 12.27kHz
Avg(1): 84.5mV
Duty(1): 25.2%
Print to disk file: PRINT_02

Fig 5.2.1 PWM output observer- 25% duty cycle

5.2.2 DUTY CYCLE 50%



Freq(1): 12.27kHz
Avg(1): 166.1mV
Duty(1): 50.0%

Fig 5.2.2 PWM output observer- 50% duty cycle

5.3 BUCK MODE (70% OF DUTY CYCLE)

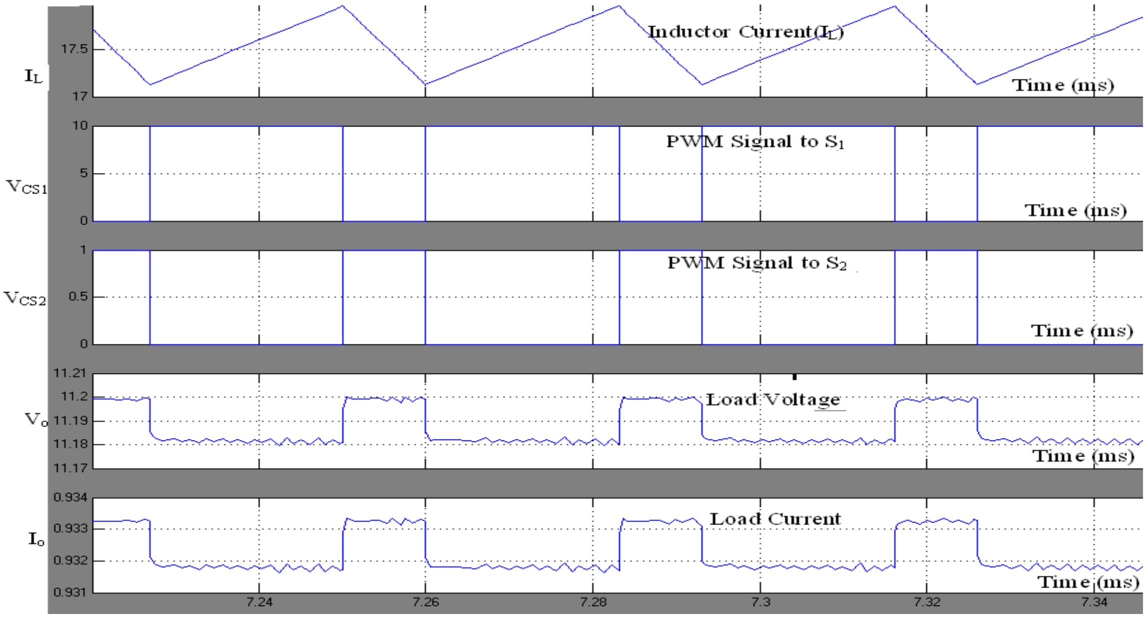


Fig 5.3 Buck Mode Waveforms

5.4 BOOST MODE (70% OF DUTY CYCLE)

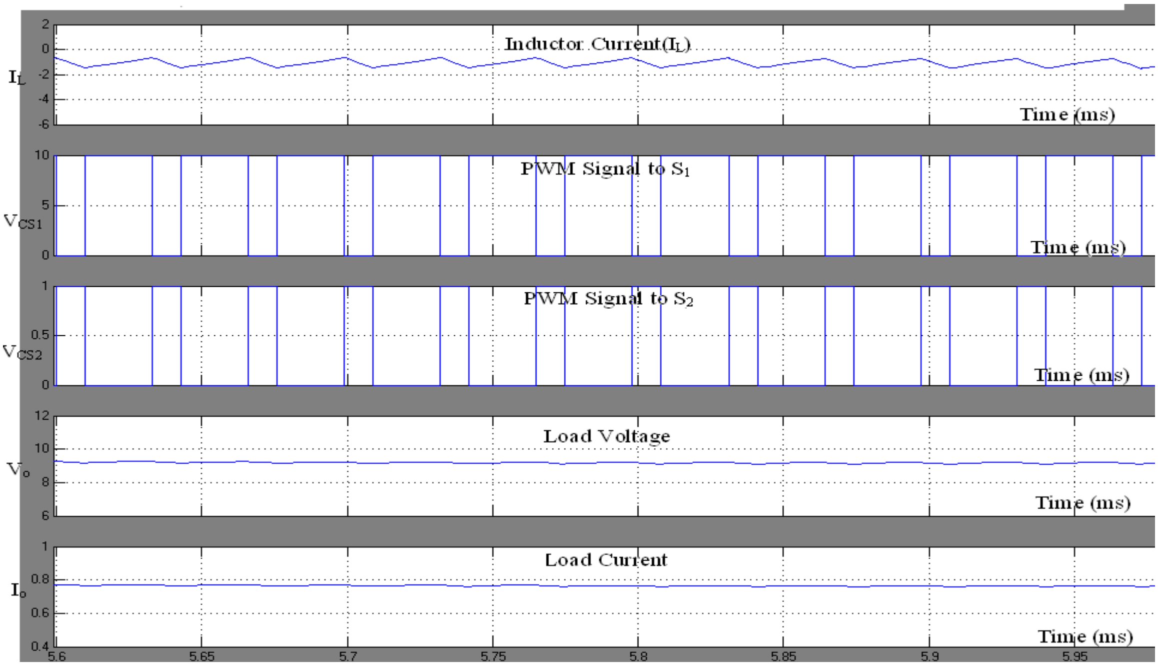


Fig 5.4 Boost Mode Waveforms

Conclusion

In this paper , the PWM signals are generated to switch the duty ratio 70% in bidirectional dc-dc converter and different modes of operation are verified in the converter. And the generation of PWM signal using XILINX FPGA has proven to be cost effective by varying the duty ratio of bi-directional dc-dc converter to 25% and 50% and the respective waveforms are evaluated using DSO.

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