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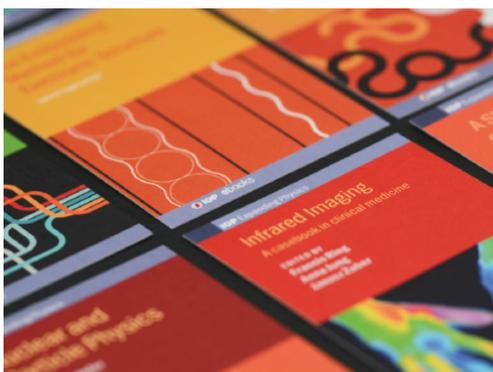
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# Process Optimization for Monolithic Integration of Piezoresistive Pressure Sensor and MOSFET Amplifier with SOI Approach

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**Abstract.** In this paper we present the design and process optimization for fabricating piezoresistive pressure sensor and MOSFET Differential Amplifier simultaneously on the same chip. Silicon On Insulator approach has been used for realizing the membrane as well as the electronics on the same chip. The amplifier circuit has been configured in the common source connection and it has been designed with PSPICE simulation to achieve a voltage gain of about 5. In the initial set of experiments the Pressure sensor and the amplifier were fabricated on separate chips to optimize the process steps and tested in the hybrid mode. In the next set of experiments, SOI wafer having the SOI layer thickness of about 11 microns was used for realizing the membrane by anisotropic etching from the backside. The piezo-resistive pressure sensor was realized on this membrane by connecting the polysilicon resistors in the form of a Wheatstone bridge. The MOSFET source follower amplifier was also fabricated on the same SOI wafer by tailoring the process steps to suit the requirement of simultaneous fabrication of piezoresistors and the amplifier for achieving MOSFET Integrated Pressure Sensor. Reproducible results have been achieved on the SOI wafers, with the process steps developed in the laboratory. Sensitivity of 270 mV /Bar/10V, with the on chip amplifier gain of 4.5, has been achieved with this process.

*Key words:* SOI wafer; MOS integrated pressure sensor; anisotropic etching.

## 1. Introduction

MEMS based sensors are becoming very popular due to their inherent advantages. Integration of these sensors with electronic circuits has the advantages of picking up less electrical noise thereby improving the precision and sensitivity of the sensor. In this paper we present an optimized process flow for the design and fabrication of monolithic integrated piezoresistive Pressure Sensor with source coupled Differential Amplifier. Polysilicon based Pressure sensors are reported in literature<sup>1</sup>. By adjusting boron doping concentration in polysilicon the temperature coefficient of resistivity (TCR) of the polysilicon resistors can be made zero<sup>2</sup>. Therefore boron doped polysilicon piezoresistors are used

in the sensor part as well as in the amplifier part. Since the polysilicon resistors are isolated from the SOI film by thermal oxide and the TCR of polysilicon resistors are made zero the resistance values will not change with respect to temperature. CMOS Integrated MEMS devices using bulk Si substrates have been reported in literature<sup>3</sup>. Since SOI based sensors and electronics shows better performance than the devices fabricated using bulk Si substrates, SOI substrates have been used to fabricate the MOSFET Integrated Pressure Sensor.

## 2. Design and fabrication of Hybrid Pressure Sensor and Source coupled Differential Amplifier

### 2.1. Fabrication of Sensor

In the pressure sensor four polysilicon resistors are connected in Wheatstone bridge form over an eleven micron silicon membrane of  $500 \times 1000 \mu\text{m}^2$  size. The bridge is unbalanced when a pressure is applied over the membrane and hence the output voltage changes. The composite mask layout used for fabrication of the sensor is shown in the Fig. 1. A SOI wafer with eleven micron thick silicon layer has been used to fabricate the Sensor. At first a thermal oxide of  $0.8 \mu\text{m}$  is grown by wet oxidation. The oxide over the SOI film is then protected by photo resist and the backside oxide is patterned using Mask # 1. The silicon is etched from the oxide patterned portion using KOH till the oxide underneath the SOI film is reached. The oxides from both the sides are removed by blanket BHF etching followed by cleaning using RCA1 and RCA2 solutions. A fresh thermal oxide of  $0.2 \mu\text{m}$  is grown by wet oxidation for isolation of the resistors from the SOI film. A  $0.6 \mu\text{m}$  thick polysilicon is deposited using LPCVD technique at  $620 \text{ }^\circ\text{C}$  followed by annealing at  $1000 \text{ }^\circ\text{C}$  for an hour. The polysilicon is implanted using boron source at  $80 \text{ KeV}$  energy with a dose of  $1.5 \times 10^{15} \text{ cm}^{-2}$ . The wafer is annealed at  $950 \text{ }^\circ\text{C}$  for 30 minutes and the polysilicon is patterned to define the four piezoresistors using Mask # 2. Aluminium metallization is done and patterned using Mask # 3. The fabricated devices are diced and packaged in TO39 header.

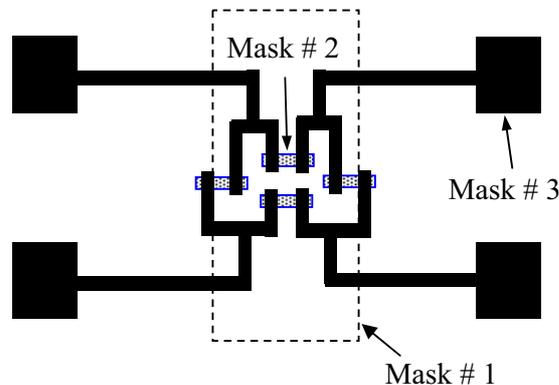


Fig.1. Composite mask layout of pressure sensor

### 2.2. Fabrication of Differential Amplifier

A source coupled amplifier has been used for amplifying the sensor output signal. P-SPICE simulations are done by considering  $500 \text{ mV}$  threshold voltage,  $50 \text{ nm}$  gate oxide for the MOSFET with a  $10 \text{ V}$  supply to the drain. The drain and source resistance values have been designed by simulation for achieving a voltage gain of 5. The drain and source resistance values are found to be  $10 \text{ K}\Omega$  and  $4 \text{ K}\Omega$  respectively for a Differential mode gain of 5. The composite mask layout used to fabricate the differential amplifier is shown in Fig. 2. A SOI wafer having SOI film thickness of  $0.6 \mu\text{m}$  with  $1\text{-}10 \Omega\text{-cm}$  resistivity, buried oxide thickness of  $0.5 \mu\text{m}$  and p-substrate thickness of  $550 \mu\text{m}$

is used to fabricate the differential amplifier. The wafer is cleaned and lithography is done using Mask #1 to define the silicon islands. A 50 nm thick gate oxide is grown by dry oxidation at 1000 °C. A 0.6 μm thick polysilicon is deposited using LPCVD technique at 620 °C. The polysilicon is implanted using boron source at 80 KeV with a dose of  $1.5 \times 10^{15} \text{ cm}^{-2}$  and annealed at 950 °C for 30 minutes. The polysilicon is patterned using Mask # 2 to define resistors and the gate regions of the MOSFETs. A 0.3 μm thick PECVD oxide is deposited and annealed at 850 °C for 20 minutes and patterned using Mask # 3 to open windows for phosphorous diffusion of source, drain and gate poly regions. The Phosphorous diffusion is carried out using  $\text{POCl}_3$  source at 950 °C for 30 minutes. A 0.1 μm thick PECVD oxide is then deposited and annealed at 850 °C for 20 minutes and patterned using Mask # 4 to define contact opening for resistors, source and drain regions. This is followed by Aluminium metallization and patterning using Mask # 5. The device is characterized to estimate the gain of the amplifier in differential mode, common mode and the results are shown in Fig. 3. The differential mode gain of the amplifier is 4.6 and the output of the amplifier is linear up to an input of 500 mV. The common mode gain and the common mode rejection ratio of the amplifier are 0.02 and 230 respectively.

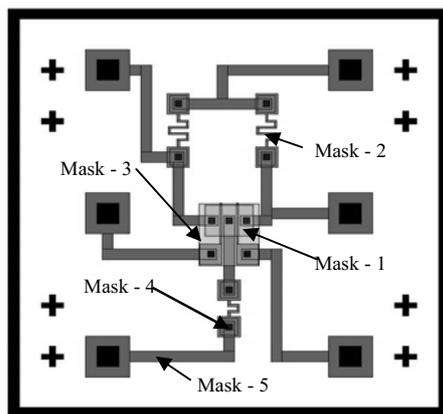


Fig. 2. Composite mask layout of Differential Amplifier

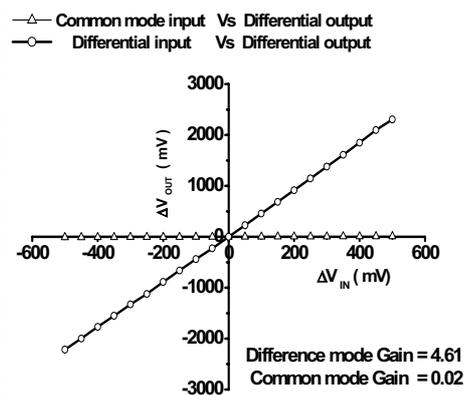


Fig. 3. Test results of Differential amplifier

### 2.3. Testing of Pressure Sensor and Differential Amplifier in Hybrid mode

The packaged Pressure Sensor and the amplifier are connected in hybrid mode as shown in Fig. 4. The Pressure Sensor is mounted on a specially fabricated jig to apply pressure. The output voltage of the sensor is given to the differential amplifier input using external wire connections.

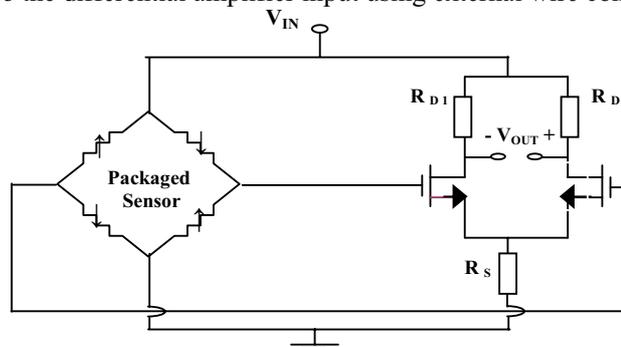


Fig. 4. Differential amplifier and Pressure Sensor connected in hybrid mode

A known amount of pressure is applied from a nitrogen cylinder to the pressure sensor. A 10 V supply is given to both the sensor input and the drain supply of the differential amplifier. The measured voltages at the sensor output and differential amplifier output up to 8 bar pressure are shown in Fig. 5. The offset voltage at the differential amplifier output is adjusted to zero by connecting an external resistor across one of the drain resistors. Sensitivity of 180 mV/Bar/10V, with the amplifier gain of 4.5 has been achieved with this pressure sensor device connected with the differential amplifier in hybrid mode.

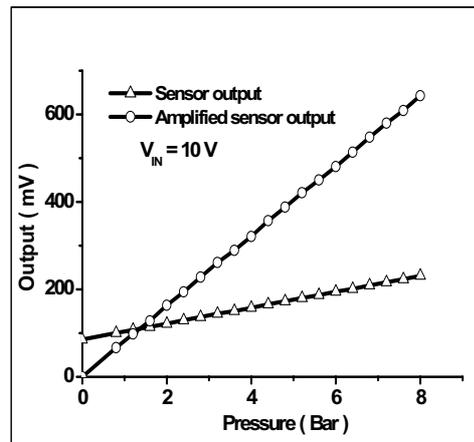


Fig. 5. Test result of Pressure Sensor Connected with Differential Amplifier in Hybrid mode

### 3. Design and fabrication of Monolithic Integrated Pressure Sensor and Differential Amplifier

By considering the process flow in the hybrid mode an optimized process flow is found and used to fabricate the Integrated Pressure Sensor device. The necessary masks have been designed using L-Edit software. A SOI wafer having a SOI film thickness of 11  $\mu\text{m}$  with 1-10  $\Omega\text{-cm}$  resistivity, buried oxide thickness of 0.5  $\mu\text{m}$  and p-substrate thickness of 285  $\mu\text{m}$  has been used to fabricate the device. The wafer is cleaned and a thermal oxide of 0.8  $\mu\text{m}$  is grown by wet oxidation. The oxide on the SOI film is protected and the oxide on the backside of the wafer is patterned and Si is etched from the oxide patterned portion using KOH till the oxide underneath the SOI film is reached. The oxides from both the sides are removed by blanket BHF etching followed by cleaning using RCA1 and RCA2 solutions. A 0.6  $\mu\text{m}$  thick field oxide is grown by wet oxidation followed by patterning to define the active area for fabrication of the MOSFETs. A 50 nm thick gate oxide is then grown by dry oxidation. This is followed by a 0.6  $\mu\text{m}$  thick polysilicon deposition using LPCVD technique at 620  $^{\circ}\text{C}$ . The polysilicon is implanted with boron source at 80 keV with a dose of  $1.5 \times 10^{15} \text{ cm}^{-2}$  and annealed at 950  $^{\circ}\text{C}$  for 30 minutes. The polysilicon is patterned to define the resistors for sensor and the amplifier as well as the gate poly for the MOSFETs. A 0.3  $\mu\text{m}$  thick PECVD oxide is then deposited and annealed at 850  $^{\circ}\text{C}$  for 20 minutes and patterned to allow phosphorous diffusion in the source, drain and gate poly regions of the MOSFET. The Phosphorous diffusion is carried out using  $\text{POCl}_3$  source at 950  $^{\circ}\text{C}$  for 30 minutes. A 0.1  $\mu\text{m}$  thick PECVD oxide is then deposited and annealed at 850  $^{\circ}\text{C}$  for 20 minutes and patterned to define contact opening for resistors, source and drain regions. This is followed by Aluminium metallization and patterning. The final cross-sectional view of the Integrated Pressure Sensor is shown in Fig. 6.

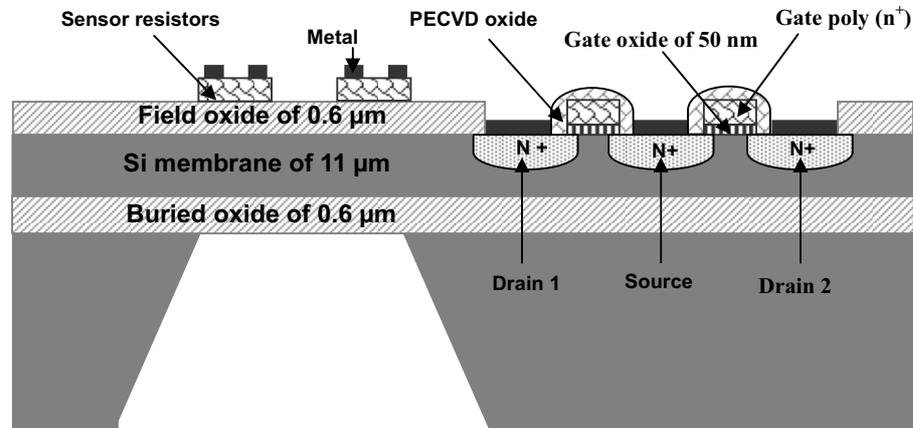


Fig. 6. Schematic Cross-sectional view of MOSFET Integrated Pressure Sensor.

#### 4. Results and Discussions

The fabricated devices are diced and packaged in TO39 header. The packaged device is mounted in a jig and a known amount of pressure is applied from a nitrogen cylinder. An input of 10 V is given to both the sensor and the drain supply of the differential amplifier. The measured voltages at the sensor output and differential amplifier output up to 7 bar pressure are shown in Fig. 7. The offset voltage at the differential amplifier output is adjusted to zero by connecting an external resistor across one of the drain resistors. Sensitivity of 270 mV/Bar/10V, with the on chip amplifier gain of 4.5 has been achieved with this process. Reproducible results have been achieved with the process developed in our laboratory. A SOI wafer with thin SOI film instead of 11  $\mu\text{m}$  may be used to get a fully depleted MOSFET for the amplifier part, which will give the full advantage of SOI structure.

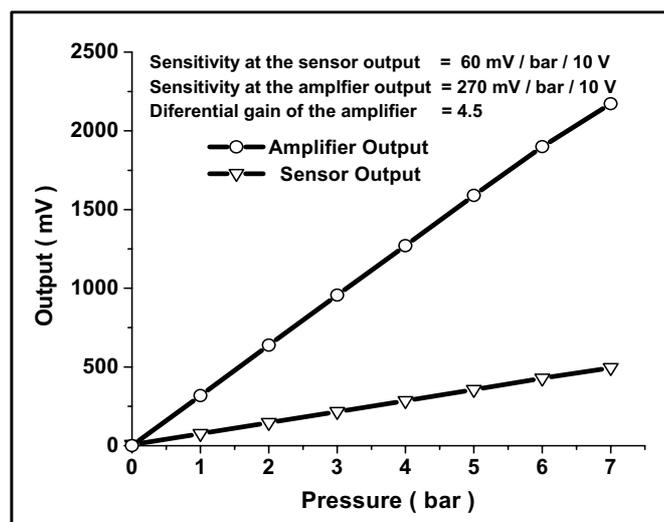


Fig. 7. Pressure Vs Output Voltage of the packaged Integrated Pressure Sensor

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