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Nanosecond threshold switching of $GeTe_6$ cells and their potential as selector devices

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Time-resolved threshold switching characteristics including transient parameters such as delay time and holding voltage are reported for a nanoscale $GeTe_6$ Ovonic threshold switching (OTS) device. The voltage dependence of the threshold switching process has been studied, revealing switching in less than 5 ns in the fastest case. A constant holding voltage is observed for the different voltage pulses applied, which is an indicative for a stable *on* state in the amorphous phase. In addition, the potential of $GeTe_6$ devices as OTS selectors is validated. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3700743]

Phase change memory (PCM) offers promising attributes for a high-speed non-volatile electronic memory. It is therefore considered to be a potential candidate for the replacement of conventional flash memories in the next decade.[1,2] Hence, in recent years tremendous technological efforts have been devoted to improve the reliability and performance of PCM devices in terms of programming characteristics, integration issues,[3,4] and structural stability.[5,6] Furthermore, several types of PCM architectures have been developed to realize a cost-effective high-density memory.[7,8] The device density in the conventional memory array is essentially determined by the selector which is frequently a thin diode.[8] Recently, a promising selector based on Ovonic threshold switching (OTS) properties[9] in chalcogenide glasses has been demonstrated in a stackable cross-point PCM device.[10] In this type of architecture, each memory bit is formed by vertically integrating a phase change memory element with an OTS selector consisting of a thin amorphous chalcogenide material. The OTS material therefore provides the same physical and electrical scaling properties as PCM devices.[10] In contrast to common complementary metal-oxide semiconductor (CMOS) selection circuits, the OTS device must not be fabricated on the silicon substrate. Thus, the vision of a high-density, three-dimensional memory can be realized via stacking of multiple layers of memory arrays. This approach promises better scalability, improves array-efficiency, and is even compatible with CMOS circuits.[10] The OTS selector acts as an electronic switch to access the adjacent memory bit upon application of appropriate voltage pulses. To select one single cell, a voltage pulse has to be applied to the selected column and row. The selected cell is accessed through the OTS, which performs threshold switching to access the PCM memory. Disturbance of adjacent memory cells (cross-talk) is avoided, since the voltage drop at their OTS selector is below the threshold voltage.

In recent years, research interest has therefore focussed on understanding threshold switching to optimize OTS selector devices. Threshold switching is known to occur in chalcogenide glasses when a critical electric field E_{th} (or threshold voltage V_{th}) is applied. Then the device switches rapidly from a highly resistive *off* state to a highly conducting dynamic low resistive *on* state. The device remains in the *on* state until the applied voltage falls below a minimum voltage called holding voltage V_h. Subsequently, the device reverts back to the initial highly resistive *off* state. Hence the OTS device is characterized by a highly conducting *on* state and a highly resistive *off* state. The highly resistive *off* state electrically isolates individual PCM cells.[10] Applying the threshold voltage to the OTS device hence enables addressing the adjacent memory cell and subsequently writing or erasing of a bit. The switching dynamics of the OTS define an upper limit for the speed of memory. Therefore, the characteristics of the OTS device including the transition kinetics are essential for the design and the optimization of programming schemes.

The initiation of threshold switching has been reported[11] to proceed with a finite delay time (t_d). The transient effects associated with threshold switching have even been shown to be voltage dependent.[5,11,12] It has also been demonstrated that the threshold switching process is not accompanied by a massive structural rearrangement such as crystallization.[5,11] Nevertheless, there is very little information available regarding the ultrafast kinetics of the switching process. This is a serious deficiency if one is interested in high-speed memories.

Hence, we have studied time-resolved nanosecond switching processes and their voltage dependence in $GeTe_6$ devices. Threshold switching investigations on the nanoscale range require an advanced experimental setup. In particular, for a reliable exploration of speed limits of an OTS device, a high frequency impedance match is essential. For the time-resolved analysis, a fast pulse generator and oscilloscope are employed with a custom-built contact board including a low noise amplifier in close proximity to the device under test. The pulse generator allows voltage pulses down to a plateau length of 1 ns and has a rise/fall time of 750 ps. Nevertheless, the amplifier and the capacitances inherent to the setup limit the minimum current pulse length to 5 ns. OTS devices have been fabricated in the classical bottom heater geometry.[3] A titanium nitride (TiN) heater with a diameter of 60 nm and a

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resistance of approximately 2 kΩ is embedded in an isolating silicon nitride layer. Subsequently, the heater is covered by a 20 nm thick $GeTe_6$ layer deposited from a stoichiometric target by DC magnetron sputtering. Finally, a 3 nm titanium adhesion layer and a 20 nm thick TiN top electrode layer have been sputter-deposited without breaking the vacuum. The sample was patterned using optical lithography.

The threshold switching properties of several OTS devices were characterized in the as-deposited amorphous phase. It is important to note that optimization of input voltage pulses is essential for the precise measurement of transient parameters that are associated with OTS behavior. For instance, the delay time is a measure of the elapsed time prior to the onset of the threshold switching event. This time interval can only be obtained precisely by applying pulses with a rather steep leading edge. On the other hand, a significantly longer trailing edge is employed to precisely measure the holding voltage, i.e., the voltage where the device current cut-off occurs. Therefore for the present investigation, voltage pulses with a fast leading edge of 1 ns, a plateau time of 100 ns, and a trailing edge of 100 ns are utilized.

Fig. 1 shows time-resolved current-voltage characteristics and threshold switching behavior of a $GeTe_6$ OTS device. The applied voltage pulse V_a depicted (black color) possesses a pulse height of 1.60 V with a leading edge of 1 ns and a plateau length/trailing edge of 100 ns, respectively. As can be seen, the device remains in the highly resistive *off* state with a very low device current I_d (~1 μA, red color) during the first 40 ns after application of the voltage pulse. Thereafter, I_d increases drastically and the device switches rapidly from a low conducting highly resistive *off* state (80 ± 10 MΩ) to a highly conducting dynamic low resistive *on* state (3 ± 1 kΩ). The event of threshold switching is also evidenced by a snap-back in the device voltage V_d (green color). It is noteworthy that the device remains in this well-conducting state until the applied voltage is reduced to the holding voltage V_h (~0.70 V), where the device current is cut-off. Below V_h, the device returns to the highly resistive *off* state. The OTS behavior and *on-off* transition were found to be reproducible for more than 500 voltage pulses.

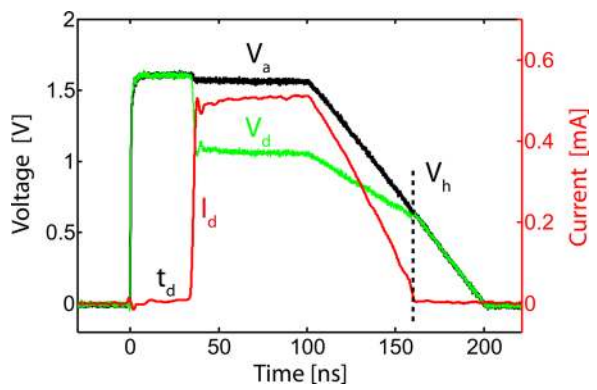

FIG. 1. Time-resolved measurement of threshold switching characteristics of $GeTe_6$ device for the applied voltage pulse V_a of 1.60 V (1 ns rise time, 100 ns plateau time and trailing edge, respectively (black color)), as well as the measured device voltage V_d (green color) and the device current I_d (red color). V_h denotes the holding voltage below which the device returns to the high resistance *off* state.

The *on-off* switching dynamics of an OTS device can limit the programming speed of memory cells. Hence, a quantitative measurement of the delay time and *on-off* characteristics of OTS devices is crucial. These transient effects have been reported in the literature to show a strong dependence on applied voltage.[13] In order to explore the dependency of delay time and *on-off* characteristics on pulse parameters, different voltage pulses were applied. This experiment was performed with several OTS cells and showed a reproducible dependency of transient parameters on the voltage pulse applied.

Fig. 2 depicts the device current I_d measured for the voltage pulses between 1.40 and 1.85 V. It has been observed that OTS device switches into a conducting *on* state with a delay time (time elapsed up to the onset of switching) of approximately 60 ns at a critical voltage of 1.60 ± 0.02 V ($E_{th} \sim 80$ V/μm), below which the device remains in the *off* state. Both the delay time and the holding voltage are deduced from these measurements and are plotted in Fig. 3. A clear trend is observed for the delay time t_d upon increasing V_a as shown in Fig. 3(a). Td rapidly decreases to < 5 ns, which corresponds to the limit of the set-up. Hence these results demonstrate that threshold switching can take place in $GeTe_6$ within 5 ns.

The stability of the *on* state of an OTS device can be characterized by the dependence of the holding voltage on the applied voltage pulse, as shown in Fig. 3(b). The holding voltage is fairly constant upon the variation of the applied voltage pulse. At the same time, the current flowing through the device in the *on* state increases by a factor of 0.6 upon increasing V_a from 1.60 to 1.85 V. This implies that the local amorphous region is not modified by the different *on* state currents.[14] The *on* state current (~650 μA) of the OTS device is found to be high enough to serve as the *reset* current

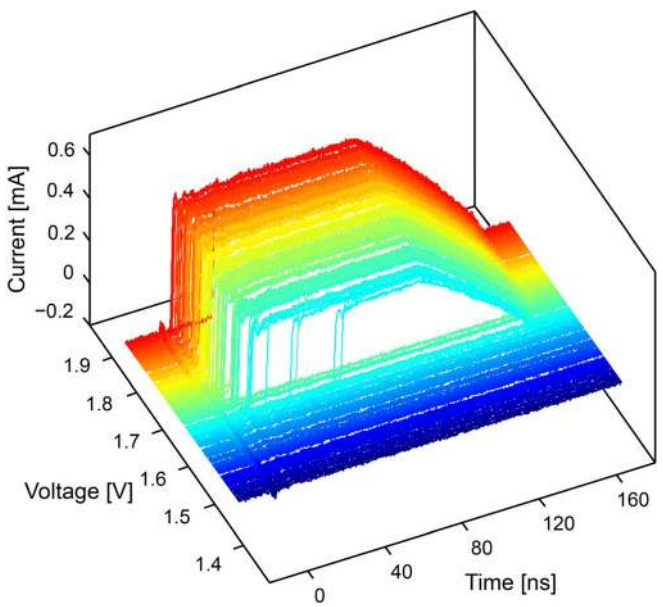

FIG. 2. Time-resolved measurement of the device current I_d for voltage pulses ranging from 1.40 to 1.85 V. The overlay of I_d reveals the dependency of transient parameters such as delay time on the voltage pulse. The height of the applied voltage pulse is color coded. This viewgraph demonstrates the pronounced dependence of the delay time upon the height of the voltage pulse.

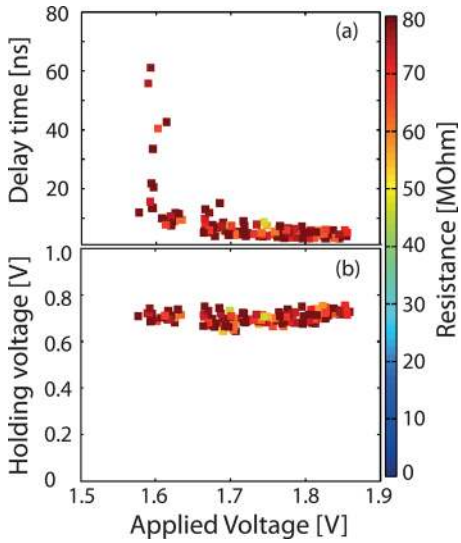

FIG. 3. Dependence of delay time t_d (a) and holding voltage V_h (b), on the applied voltage. The different colors represent the device resistance before the threshold switching event.

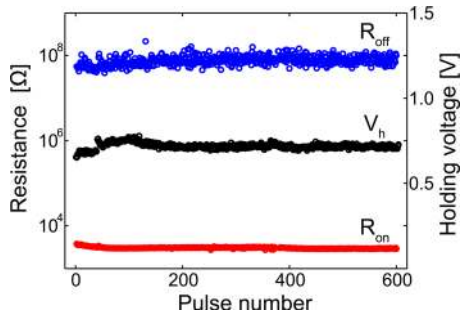

FIG. 4. The transition from a highly resistive *off* state to a highly conducting *on* state in the amorphous phase is depicted for a series of switching events. A constant holding voltage confirms the stability of the amorphous *on* state (black color). These cycling measurements demonstrate the stability of the *on* and *off* resistance upon multiple threshold switching processes. The result of numerous switching events is highly reproducible as well ($R_{off} = (80 \pm 10$ MΩ), $R_{on} = (3 \pm 1$ kΩ), and $V_h = 0.70 \pm 0.02$ V).

for various PCM cell structures.[8] Therefore, the OTS *on* state current can be utilized to induce the crucial phase-change from the *set* to the *reset* state in memory cells. The *set* and *reset* state of PCM refers to the low and high resistance state, respectively. Creating the highly resistive *reset* state is accomplished by local melting and rapid quenching of the phase change material, which leads to an amorphous phase. This transformation is the most power consuming process in non-volatile memories employing PCMs. On the other hand, the transition from the *reset* to *set* state needs a combination of threshold and memory switching which finally leads to the formation of the low resistive crystalline state in the PCM cell. To identify the state of the memory cell, a much lower read voltage of ~200 mV is used.

The theoretical models described in the literature which explain threshold switching are either based on the generation and recombination of charge carriers[15,16] or field induced crystallization.[17] In these models, charge transport in the amorphous phase is either by hopping or trap limited band transport. Until now, no direct experimental evidence has been demonstrated that has allowed for the verification of a single theory. Within this work, we provide experimental results which could help to improve our understanding of threshold switching properties and their relaxation behavior. The data presented in Figs. 2 and 3 unequivocally demonstrate that the holding voltage of $GeTe_6$-based OTS devices is fairly constant for the range of applied voltage pulses. Hence, these results could directly be verified by threshold switching models simulating the relaxation behavior.

In order to further investigate the stability and repeatability of the OTS device performance, a series of experiments has been carried out. Fig. 4 shows the reproducibility of the switching between the highly resistive *off* state and the low resistive *on* state of the amorphous $GeTe_6$ OTS device for more than 600 pulses ($V_a = 1.60$ V, 1 ns of rise/fall time, 100 ns of plateau time). The OTS device electronically switches between *off and on* states in a stable fashion as can be seen from the stable resistances. The holding voltage also remains fairly stable upon multiple switching cycles as shown in Fig. 4, as well. In a previous study for an $Ge_{25}Te_{75}$ alloy, the threshold voltage has been found to decrease after more than 100 applied voltage pulses,[18] which has been attributed to the partial crystallization of the amorphous region. Therefore, the material of choice for a stable OTS selector is characterized by its ability to prevent crystallization during operation. Hence, it is mandatory that the *on-off* switching stability of the chalcogenide glass remains constant for long operating times and repeated use. It has been reported in the literature[19] that $GeTe_6$ is a good glass former, which exhibits slow crystallization with a crystallization time of more than 100 μs. Hence crystallization induced by ns pulses is impossible. Nevertheless, in the present experiments, an increase in the threshold voltage is observed after the application of more than 600 pulses. This could be due to a change in the local structure of the amorphous state caused by thermal annealing by the current in the *on* state as well as additional heat produced by the TiN heater, embedded below the active material. Further improvements on the sample preparation and device structure might help to advance reliability and performance characteristics of the OTS device.

In summary, we have demonstrated time-resolved electrical switching experiments on $GeTe_6$-based OTS devices which show threshold switching as fast as 5 ns. A strong dependency of delay time on the applied voltage is observed. The stability of the *on* state has been testified by a constant holding voltage and *on* state resistance. Hence, this OTS selector can enable high-density, stackable cross-point phase-change memory devices for future random access memory and solid state storage applications.

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