Received 24 December 2019; revised 13 February 2020; accepted 8 March 2020. Date of publication 13 March 2020; date of current version 27 March 2020. The review of this article was arranged by Editor N. Collaert.

Digital Object Identifier 10.1109/JEDS.2020.2980633

Impact of Source to Drain Tunneling on the Ballistic Performance of Si, Ge, GaSb, and GeSn Nanowire p-MOSFETs

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ABSTRACT We investigated the effect of material choice and orientation in limiting source to drain tunneling (SDT) in nanowire (NW) p-MOSFETs. Si, Ge, GaSb, and $Ge_{0.96}Sn_{0.04}$ nanowire MOSFETs (NWFETs) were simulated at a scaled gate length (L_G) of 10 nm, using rigorous ballistic quantum transport simulations. To properly account for the non-parabolicity and anisotropy of the valence band, the k·p method was used. For each material, we simulated a set of six different transport/confinement directions, at a fixed OFF-state current (I_{OFF}) of 100 nA/μm and supply voltage $V_{DD} = -0.5$ V to identify the direction with the highest ON-current (I_{ON}). For Ge, GaSb, and GeSn [001]/110/$\bar{1}$10 oriented NWFETs, with [001] being the direction of transport and 110, $\bar{1}$10 being the directions of confinement for the nanowire, showed the best ON-state performance, compared to other orientations. Our simulation results show that, despite having a higher percentage of SDT in OFF-state than silicon, GaSb [001]/110/$\bar{1}$10 NWFET can outperform Si NWFETs. We further examined the role of doping in limiting SDT and demonstrated that the ON-state performance of Ge and GeSn NWFETs could be improved by reducing the doping in the source/drain (S/D) extension regions. Our simulation result show that with properly chosen channel transport orientation and S/D doping concentration, performance of materials with high hole mobility can be optimized to reduce the impact of SDT and provide a performance improvement over Si-channel based p-MOSFETs.

INDEX TERMS SDT, k · p method, nanowire MOSFETs, quantum transport simulations, NEGF, GaSb, GeSn.

I. INTRODUCTION

Increased source to drain tunneling (SDT) leakage in devices with short channel length can become a significant roadblock in scaling down transistor dimensions [1]–[3]. III-V semiconductors with high electron mobility like InGaAs, although regarded as promising candidates for future generation n-MOSFETs [4] are more susceptible to SDT leakage due to their lower transport effective mass (m^*_{trans}). III-V channel-based p-MOSFETs can be more immune to SDT leakage in OFF-state compared to their n-channel counterparts at scaled gate lengths due to their higher m^*_{trans} compared to electron m^*_{trans}. Devices based on III-V materials like GaSb are being actively explored as a potential candidate to replace Si as a channel material for the future generation of p-MOSFETs [5], [6]. At the same time, the anisotropic nature of the valence band makes the performance of scaled p-MOSFET devices strongly dependent on the direction of transport/confinement [7]. Hence it may be possible to engineer hole effective masses in materials with higher hole mobility compared to Si, to limit SDT and improve the device performance. Germanium used to have the highest bulk hole mobility among all the elemental group IV and III-V semiconductors [4]. Recently, GeSn alloy based p-channel MOSFETs have achieved higher effective hole mobility compared to pure Ge based FETs [8], [9]. Also, conventional mobility enhancement techniques like using embedded source/drain (S/D) stressor or strained capping layers are becoming less effective at very small gate pitches [10].

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Hence, to enable device scaling with performance improvements over conventional strained-Si based p-MOSFETs, it is essential to explore the relative merits/demerits of MOSFETs based on alternate channel materials. Nanowire MOSFETs (NWFETs) due to their ability to provide the ultimate electrostatic control of the channel by the gate are regarded as a promising device architecture to continue scaling [11]. Hence in this paper, we have carried out a comparative analysis of the ballistic performance of Si, Ge, GaSb, and $Ge_{0.96}Sn_{0.04}$ (GeSn) NWFETs, to determine their suitability as a channel material for the future generation of p-MOSFETs.

A lot of studies have focussed in assessing the performance of Si, Ge, and III-V nanowire n-MOSFETs in the presence of SDT [2], [12]–[14]. But a similar study involving III-V materials along with Si, Ge for nanowire p-MOSFETs has not been carried out. In [15], some III-V materials alongside Si, Ge NWs have been considered. The authors have focussed on the ability of these materials in blocking SDT current for n- and p-NWFETS, but ON-state performance of these materials have not been evaluated. Other studies involving nanowire p-MOSFETs have only considered Si and Ge as channel materials and have been carried out either at longer gate lengths [14], with smaller SDT current component or have employed a semiclasical top of the barrier (ToB) model [16], which does not account for SDT. In [7], [17] ballistic performance of Si NWFETs has been evaluated in different transport orientations using the ToB model. In [3] an optimized range of m^*_{trans} has been provided, which has been treated as a material independent quantity, to optimize device performance for sub-12 nm nodes. In [3] however, transport was treated using a single band effective mass (EM) model. The EM model cannot account for the non-parabolic and coupled nature of valence bands [18]. Recently, Chang *et al.* [19] have analyzed the ballistic performance of III-V double-gate p-MOSFETs using the ToB semiclassical transport model.

In this work, we perform ballistic quantum transport simulations using the $k \cdot p$ method, to analyze the impact of SDT on the performance of nanowire p-MOSFETs. A comprehensive analysis of the effects of the valence band dispersion relations, resulting from the use of different channel materials and crystallographic orientations will provide essential guidelines in designing sub-10 nm p-MOSFETs. We have performed rigorous ballistic quantum transport simulations of NWFETs with Ge, GaSb, and GeSn as the channel materials and compared their performance with Si NWFETs. For these materials, we have attempted to identify the transport directions which can minimize the OFF-state SDT without compromising too much on the ON-state performance.

The rest of the paper is organized as follows. We briefly summarize the simulation approach in Section II. In Section III, we analyze the ballistic performance of all the four materials with different transport orientation and source/drain doping concentrations. We also investigate the behavior of injection velocity and quantum capacitance in the ballistic limit. Finally, we conclude the paper in Section IV.

TABLE 1. Summary of NW axial orientation and directions of confinement.

NW axial orientation	Transport direction (x)	Confinement directions (y/z)
[100]	100	010/001
[110]	110	$\bar{1}10/001$
[111]	111	$0\bar{1}1/\bar{2}11$
[001]	001	$110/\bar{1}10$
$[0\bar{1}1]$	$0\bar{1}1$	$\bar{2}11/111$
$[\bar{2}11]$	$\bar{2}11$	$0\bar{1}1/111$

II. APPROACH

To investigate the effect of SDT on the performance of different channel materials, we adopt the following methodology,

1) All the materials have been compared at a fixed gate length of $L_G = 10$ nm. The gate length is chosen as per ITRS 2015 [20] guidelines. Based on this choice of L_G, the dimensions of the cross-section, viz, 5 nm $\times$ 5 nm and equivalent oxide thickness (EOT) $\sim$ 0.65 nm are chosen, to ensure $L_G > 5\lambda$ for all the materials considered in this work, with λ being the natural length of the device [21]. Since our aim is to optimize m^*_{trans} to limit SDT, by varying channel material and orientation, rather than by changing device geometry, the dimensions of the device cross-section were kept constant throughout all the simulations.
2) We also analyzed the impact of channel transport orientation in minimizing SDT. For each material, NWFETs with six different transport orientations were simulated, to identify the orientation providing the highest ON-current (I_{ON}). For a fair comparison, OFF-state current (I_{OFF}) for each orientation was made 100 nA/μm by adjusting the gate work function. Current values are shown after normalizing the current by the nanowire device perimeter.
3) The role of doping in minimizing SDT and improving I_{ON} has been examined for Ge and GeSn NWFETs.

We have solved self-consistently, the 3D-Poisson's equation and Schrödinger's equation within the non-equilibrium Green's function (NEGF) formalism, to analyze the effect of NW bandstructure and electrostatics on the overall performance of NWFETs. A schematic of NWFETs simulated in this study is shown in Fig. 1(a). The summary of NW transport directions simulated, with their directions of confinement is given in Table 1. Hereafter, for brevity, we denote different NWFETs using their direction of transport. For materials with indirect bandgaps, the 6 band $k \cdot p$ method provides an accurate description of valence bands around the Γ point [23]. Hence for Si, Ge and GeSn, the 6 band $k \cdot p$ method has been used. For GaSb with a direct bandgap, we have used the 8 band $k \cdot p$ method.

To reduce the computational load associated with the solution of NEGF equations, we first transformed the device Hamiltonian from real space to reciprocal space [18]. Since the Hamiltonian in reciprocal space was still too expensive to be used in transport simulations, the mode-space (MS) Hamiltonian was constructed, which was then used

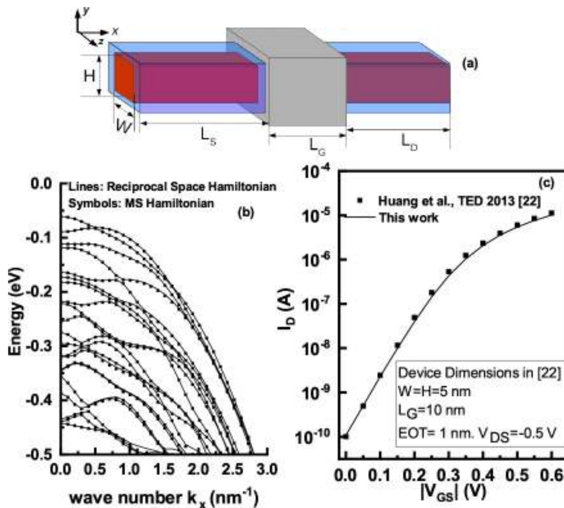

FIGURE 1. (a) Schematic of the simulation domain of NWFETs used in this work. (b) Hole sub-bands of Si [100] nanowire with 5 nm × 5 nm area of cross-section, obtained from reciprocal space Hamiltonian (Solid lines) and mode space Hamiltonian (Symbols). (c) Drain current (I_D) vs gate-source voltage (V_{GS}) characteristics for silicon NW pFET. Benchmarked results of Si NWFET to compare simulation approach. Our results (solid line) and [22] (symbols). Simulations in (c) were carried out at drain-source voltage (V_{DS}) of −0.5 V.

in NEGF simulations. For the 6 band $k \cdot p$ method, the MS Hamiltonian was constructed following the approach outlined by Huang *et al.* in [22]. Similar to [22], we constructed the MS Hamiltonian by sampling the modes at the Γ point first (k-space sampling), and then by performing an energy space sampling at an energy of $E = E_{top} - E_{int}$, where E_{top} is the energy at the top of the valence band edge and E_{int} is the energy interval starting from E_{top}, over which we need the bandstructure obtained from the MS approach to match the bandstructure obtained using the reciprocal space Hamiltonian. The MS transformation Hamiltonian was then constructed by combining the modes obtained by k-space sampling to those obtained by energy space sampling and ortho-normalizing the resultant matrix [22]. For GaSb with the 8 band $k \cdot p$ model, the approach proposed in [24] was used. For 8 band $k \cdot p$ method, only k-space sampling was used [24]. Spurious energy states in the MS Hamiltonian were removed by discarding modes with singular values smaller than an iteratively determined threshold value [25]. For simulating NWs with different transport/surface orientations appropriate coordinate transformations were performed [26]. Recursive Green's function algorithm [27] was used to speed up the calculation of charge density. The converged charge density was then fed to a 3D Poisson's equation solver and these sequence of steps were repeated in a self-consistent manner.

To check the validity of MS transformation, we compared the E-k relation obtained by using the MS Hamiltonian to the one obtained using the reciprocal-space Hamiltonian. The bandstructure of [100] oriented Si NW is shown in Fig. 1(b). To benchmark the NEGF simulation approach,

TABLE 2. List of material parameters used in simulation. Only parameters needed during simulation are listed.

Parameters	Si	Ge	GaSb	GeSn
γ_1	3.60	9.37	13.27	10.54
γ_2	0.67	3.01	4.97	3.38
γ_3	1.21	4.02	5.978	4.52
Δ_{so} (eV)	0.044	0.306	0.748	0.332
m_c/m_0	–	–	0.042	–
E_g (eV)	–	–	0.751	–
E_p(eV)	–	–	21.2	–

we performed simulations of a Si NWFET and compared it with a similar device in [22]; the results of benchmarking are shown in Fig. 1(c). The parameters used in simulation are given in Table 2. $\gamma_{1,2,3}$ represent the Luttinger parameters [28], [29] for a given material. Δ_{SO} is the spin-orbit splitting energy [28]. m_c is the electron effective mass in the conduction band, given in terms of the free electron mass m_0, E_g is the energy band-gap, while the parameter E_P is the energy equivalent [30] corresponding to the optical matrix element P [28]. The last three parameters in Table 2 are needed only while performing 8-band $k.p$ method simulations for GaSb NWFETs. Si parameters are taken from [29]. Luttinger parameters for Ge and GeSn are taken from [31] while parameters of GaSb are taken from [25].

In this work the impact of NW cross-section dimensions on the device performance has not been considered. For NWs with a smaller cross-section, the more accurate atomistic tight binding (TB) method can be used, with the MS transformation of TB Hamiltonian [32] performed at a relatively cheaper computational cost. The impact of NW cross-section dimension and gate length on these set of channel materials will be the subject of a future study. In this work, we have assumed ballistic transport, and the effects of phonon, surface roughness scattering and alloy scattering for GeSn NWFETs were not considered. We also note that the results presented in this work are valid in the ballistic limit since scattering has not been considered. A more detailed study taking into account various scattering mechanisms, for these set of channel materials would be necessary to determine the best channel material and transport direction in the quasi-ballistic regime.

III. RESULTS AND DISCUSSION

The dimensions of the simulated devices (indicated in Fig. 1(a)) are $L_S = L_D = 15$ nm (lengths of S/D extension regions). $L_G = 10$ nm. The dimensions of the cross-section are $W = H = 5$ nm. EOT ∼ 0.65 nm and a supply voltage of $V_{DD} = -0.5$ V were used in all simulations. Doping levels in S/D extension regions are 10^{20} cm^{-3} for Si, Ge, and GeSn NWFETs, and 5×10^{19} cm^{-3} for GaSb NWFETs. A lower value of doping in the S/D extension regions of GaSb NWFETs is chosen since it is difficult to achieve higher doping levels in III-V semiconductors [33], due to the lower solid solubility limit of dopants in III-V semiconductors compared

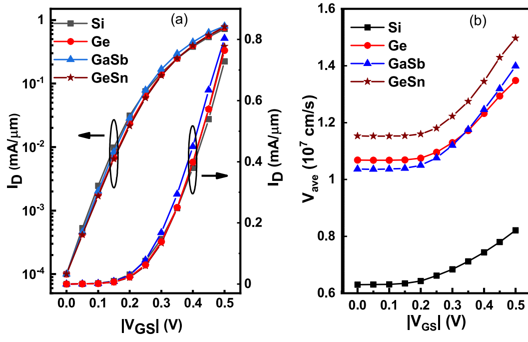

FIGURE 2. (a) $I_D - V_{GS}$ characteristics of Si, Ge, GaSb and GeSn [100] oriented NWFETs. (b) V_{ave} at the virtual source for devices in (a).

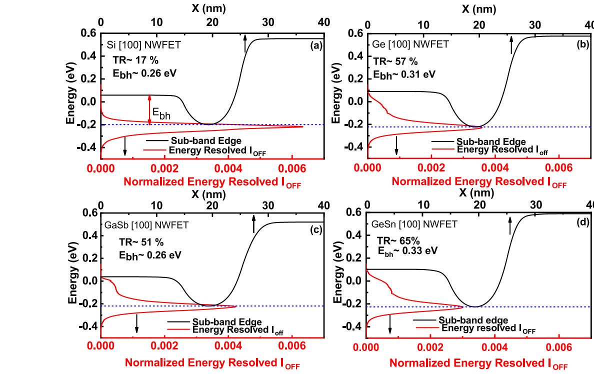

FIGURE 3. Normalized current spectrum in OFF-state for (a) Si (b) Ge (c) GaSb (d) GeSn [100] oriented NWFETs.

to group IV semiconductors. All simulations were carried out at a temperature of 300 K.

A. MATERIAL DEPENDENCE

In this subsection, we compare the ballistic performance of [100] oriented NWFETs for all the four materials. Figure 2(a) shows the drain current (I_D) vs gate-source voltage (V_{GS}) characteristics of Si, Ge, GaSb and GeSn NWFETs oriented in [100] transport direction. Si NWFET has the lowest I_{ON} due to its lower injection velocity. Figure 2(b) shows the average ballistic injection velocity (V_{ave}) [34], [35] at the virtual source. GeSn NWFET has the highest V_{ave} among all the four materials. It also has the highest component of SDT in the OFF-state. Figure 3 shows the normalized energy resolved I_{OFF} for all the materials in [100] orientation. Current values are normalized by the total I_{OFF}. Current flowing above the blue dashed lines in Fig. 3 constitutes the tunneling current. For Si NWFET, tunnel ratio (TR) defined as the ratio of current flowing by tunneling to the total I_{OFF} is ∼17%. Thus most of the current in OFF-state is due to thermionic emission over the potential barrier. GeSn NWFET on the other hand has a TR of ∼65%, highest among all the four materials. Thus the potential energy barrier height (E_{bh}) needed to achieve the same I_{OFF} in [100] oriented GeSn NWFET is higher compared to [100] Si NWFET.

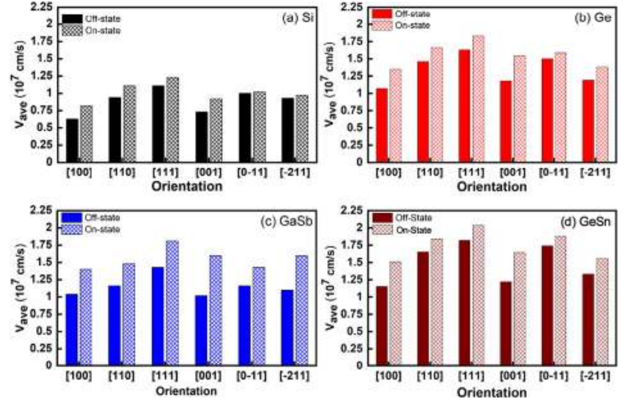

FIGURE 4. ON and OFF-state V_{ave} at virtual source for (a) Si, (b) Ge, (c) GaSb, (d) GeSn NWFETs.

TABLE 3. I_{ON} for Si, Ge, GaSb, and GeSn NWFETs with different transport orientations.

Orientation	I_{ON} (mA/um)			
	Si	Ge	GaSb	GeSn
100/010/001	0.73	0.76	0.80	0.78
110/$\bar{1}$10/001	0.84	0.74	0.80	0.69
111/0$\bar{1}$1/$\bar{2}$11	0.88	0.75	0.88	0.66
001/110/$\bar{1}$10	0.80	0.87	0.98	0.85
0$\bar{1}$1/$\bar{2}$11/111	0.80	0.70	0.82	0.62
$\bar{2}$11/0$\bar{1}$1/111	0.82	0.72	0.85	0.62

This results in lower ON-state overdrive in [100] oriented GeSn NWFET.

GaSb [100] NWFET has the highest I_{ON} among all the four materials. A lower TR ∼ 51% for GaSb NWFET compared to GeSn results in a higher ON-state overdrive. GeSn NWFET has the worst subthreshold swing (SS) initially, due to higher TR, implying degraded gate control over the channel. But once the devices start operating above the subthreshold region, the change in the slope of the $I_D - V_{GS}$ curve is steepest for GeSn NWFET. The performance of [100] oriented NWFETs is, however, sub-optimal in terms of I_{ON}. For all materials, an increase in the ballistic injection velocity, over its value in [100] oriented NWFETs results in an increased I_{ON}. However, for all materials I_{ON} doesn't increase proportionately, with an increase in the injection velocity. The orientation dependent performance variation for all the materials is discussed in the next subsection.

B. ORIENTATION DEPENDENCE

Table 3 shows I_{ON} for all materials with different orientations. Orientation dependence of V_{ave} at the virtual source is shown in Fig. 4. Both ON and OFF-state V_{ave} are shown. Irrespective of the material choice, [111] oriented NWFETs have the highest V_{ave}, while [100] oriented NWFETs have the lowest V_{ave}. Figure 5(a) shows the I_D-V_{GS} characteristics of orientations with the highest I_{ON} for each material. In the case of Si NWFETs, [111] oriented NWFET has the highest I_{ON}. The superior performance of [111] oriented Si NWFET, which has the highest V_{ave} and TR among all Si NWFETs,

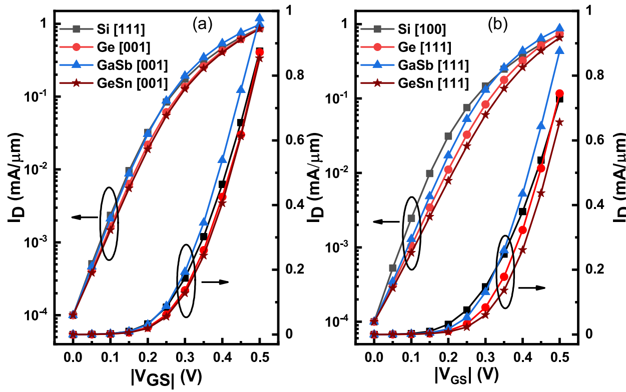

FIGURE 5. (a) $I_D - V_{GS}$ characteristics for orientations with highest I_{ON} for each material. (b) $I_D - V_{GS}$ characteristics of [111] oriented Ge, GaSb, and GeSn NWFETs compared with [100] Si NWFET.

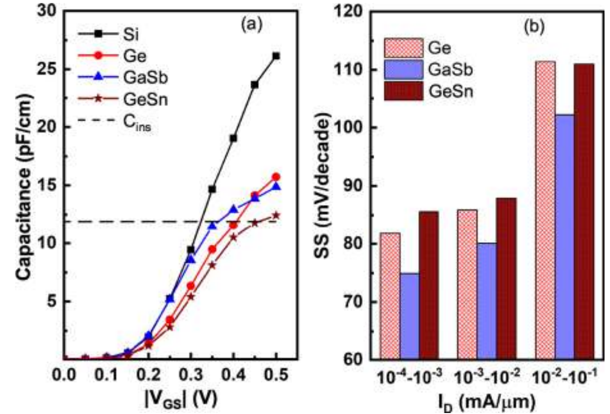

FIGURE 6. (a) Quantum capacitance vs V_{GS} for directions with highest I_{ON} for each material. (b) SS for first 3 decades of I_D for [001] oriented Ge, GaSb and GeSn NWFETs.

shows that all Si NWFETs still operate in the thermionic current component dominated regime in OFF-state.

For Ge, GaSb, and GeSn, [001] oriented NWFETs have higher I_{ON} compared to other orientations. The reason for the superior performance of [001] oriented NWFETs over [100] oriented NWFETs is their very similar V_{ave} in OFF-state to [100] oriented NWFETs, as shown in Fig. 4. This results in [001] oriented NWFETs having similar TR and SS as [100] oriented NWFETs. A similar value of TR implies that the barrier height for maintaining the same I_{OFF} is nearly identical. Similar SS also means nearly same threshold voltage (when threshold voltage is defined using the constant current method). This leads to similar ON-state overdrive voltage and almost identical values of inversion carrier density for [001] and [100] oriented NWFETs. In ON-state, however, the injection velocity for [001] oriented NWFETs is higher compared to [100] orientation. In ON-state, as k-states with higher energy are occupied, V_{ave} increases. These states have higher velocity compared to states near the $k = 0$ point [34], due to the higher gradient of the dispersion relation for the off-zone center states. The gradient of energy with respect to k for [001] oriented NWs for Ge, GaSb, and GeSn is much higher compared to [100] oriented NWFETs. Once the high energy off-zone center states are populated in ON-state, V_{ave} increases significantly for [001] NWFETs. Higher V_{ave} for [001] oriented NWFETs results in a better ON-state performance compared to [100] oriented NWFETs even though both have similar values of inversion charge density.

For [111] oriented NWFETs, the larger injection velocity (lower m^*_{trans}) results in higher SDT, and degraded gate control. Figure 5(b) shows the $I_D - V_{GS}$ characteristics of [111] oriented NWFETs, for Ge, GaSb and GeSn NWFETs. $I_D - V_{GS}$ characteristic of Si [100] NWFET, which has the lowest V_{ave} in ON and OFF-states is also shown for comparison. The degraded gate control and higher SS for [111] oriented NWFETs results in inferior performance in the sub-threshold region. The SS for the first decade of change in I_D from the I_{OFF} value, TRs along with the hole inversion density for different materials and transport direction combinations are given in Table 4. As can be seen, for all the materials [111] oriented NWFETs have the worst SS, highest TR and lowest inversion carrier density. Higher V_{ave} for [111] oriented NWFETs is not enough to compensate for the loss of ON-state overdrive due to higher SDT in OFF-state. Hence [111] oriented Ge, GaSb, and GeSn NWFETs underperform compared to [001] oriented NWFETs for these materials.

TABLE 4. SS, TR, and hole inversion density for Si, Ge, GaSb, and GeSn NWFETs with different transport orientations.

Material and Orientation	SS (mV/dec)	TR (%)	Hole Density (cm^{-1})
Si [100]	70	16.64	1×10^7
Si [111]	72	39.76	8.97×10^6
Ge [001]	82	65.97	7.89×10^6
Ge [111]	99	91.24	5.85×10^6
GaSb [001]	75	54.69	7.39×10^6
GaSb [111]	90	86.23	5.75×10^6
GeSn [001]	86	73.39	7.03×10^6
GeSn [111]	108	95.89	4.77×10^6

For comparison across materials, we show the quantum capacitance (QC) [36] as a function of V_{GS} in Fig. 6(a) for directions having the highest I_{ON} for each material. Our simulation results show that these devices operate close to the quantum capacitance limit [36]. Hence the QC values are comparable (except for Si) to the NW insulator capacitance (C_{ins}), which is calculated, taking into account the NW device geometry [37]. Ge and GaSb [001] oriented NWFETs have comparable values of QC and V_{ave} (as shown in Fig. 4). Despite this, GaSb [001] NWFET outperforms Ge [001] oriented NWFET and has the highest I_{ON} among all materials, with all different orientations considered. Ge [001] oriented NWFET underperforms compared to GaSb [001] oriented NWFET primarily due to higher OFF-state SDT and worse SS. Figure 6(b) shows the SS over the first three decades of I_D, over which the characteristics are sub-threshold like. Ge [001] NWFET has higher SS in this region due to degraded

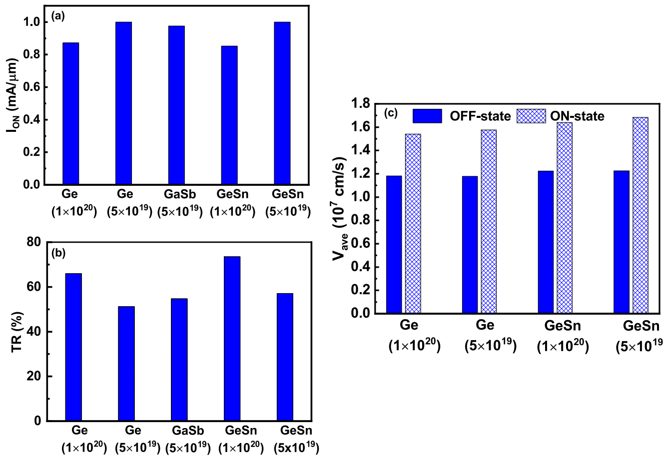

FIGURE 7. (a) Doping dependence of I_{ON} for Ge and GeSn [001] oriented NWFETs. I_{ON} for [001] oriented GaSb NWFET is also shown for comparison. (b) Tunnel ratios for devices considered in (a). (c) Impact of doping on V_{ave} at the virtual source. Doping levels in S/D extension regions in cm^{-3} are indicated within parenthesis.

gate control as a result of higher SDT. Higher SDT in Ge [001] NWFET compared to GaSb [001] oriented NWFET is partly also due to the higher doping in the S/D extension regions. SDT can be reduced by reducing the doping concentration in S/D extension regions [38]. With the same level of doping as GaSb, both Ge and GeSn NWFETs outperform [001] oriented GaSb NWFET, as shown in the next subsection.

C. IMPACT OF DOPING

In this subsection, we reduce the doping levels in the S/D extension regions of Ge and GeSn NWFETs from 1×10^{20} to 5×10^{19} cm^{-3}, to compare their performance with GaSb NWFETs at the same level of doping. [001] oriented NWFETs were simulated as they provide the highest I_{ON} for each of the three materials. Figure 7(a) shows I_{ON} for [001] oriented Ge and GeSn NWFETs with S/D doping of 5×10^{19} cm^{-3} and 1×10^{20} cm^{-3}. At the same value of S/D doping, Ge and GeSn NWFETs show marginally better ON-state performance as compared to GaSb [001] oriented NWFET. The TRs for these devices is shown in Fig. 7(b). Tunnel ratios improve considerably for both Ge and GeSn [001] oriented NWFETs at lower doping levels. The impact of lower S/D doping on V_{ave} at the virtual source is shown in Fig. 7(c). The OFF-state V_{ave} remains practically unchanged for lower doping levels in the S/D extension regions. Hence, the reduction in SDT is due to the widening of source-channel potential barrier as a result of lower doping levels in S/D extension regions [39]. A reduced doping results in a longer effective channel length [40], [41] and a wider source-channel potential barrier. This leads to a reduction in SDT current in OFF-state. Reduced SDT improves the subthreshold characteristics and also increases the ON-state overdrive voltage resulting in a higher I_{ON} for NWFETs with a lower value of S/D doping. The ON-state V_{ave} increases slightly, primarily due to enhanced ON-state overdrive voltage, which results in hole sub-bands moving more closer to the source contact Fermi level, increasing the occupation probability of the sub-bands.

Our simulation results thus demonstrate that with a proper choice of channel transport orientation and S/D doping concentration, all the three high mobility materials viz. Ge, GaSb and GeSn NWFETs for p-MOSFETs can outperform Si NWFETs, despite having a higher SDT leakage compared to Si NWFETs in the OFF-state. Materials like InAs, GaAs for n-channel MOSFETs, suffer from the density of states bottleneck and SDT leakage due to lighter electron m^*_{trans} and underperform compared to Si channel based n-MOSFETs for high performance logic devices [12], [42]. On the other hand, materials studied in this work remain attractive alternatives to Si-channel based p-MOSFETs, at this scaled gate length of 10 nm. This can be explained by examining the corresponding E-k dispersion relations for high hole mobility materials, where due to a larger hole quantization mass, valance sub-bands are more closely spaced in energy, and a large number of hole sub-bands with different hole effective masses participate in transport. Also, a more significant degree of anisotropy of valance sub-bands compared to conduction band provides greater flexibility in tuning transport properties by varying the channel transport orientation. These properties, along with a proper choice of S/D doping concentration, make it possible to optimize the performance of devices based on high hole mobility channel materials and makes them potential candidates to replace strained-Si channel based devices in the future generation p-MOSFETs.

IV. CONCLUSION

In this work, we have for the first time, carried out a comprehensive analysis of the impact of source to drain tunneling (SDT) on the performance of GaSb and GeSn NWFETs. Comparison of Ge, GaSb, and GeSn NWFETs with Si NWFETs shows that unless devices with proper channel orientation and S/D doping concentration are chosen, SDT can be a significant performance limiter for materials with high hole mobility. At the scaled gate length of $L_G = 10$ nm, while Si NWFETs still operate in the thermionic current dominated regime, other materials operate in the tunneling current dominated regime in OFF-state (tunnel ratio $> 50\%$). Our ballistic simulation results show that the amount of SDT for each material is strongly dependent on the nanowire transport/confinement directions at this gate length. [111] oriented NWFETs despite having the highest V_{ave} among all orientations for all the high mobility materials have lower I_{ON} due to a higher SDT leakage in OFF-state. Furthermore, SDT though, has a significant impact on the ON-state performance; it is not the sole factor determining the ON-state performance of devices. For optimizing the device performance, one needs to strike a balance between lower V_{ave} and higher SDT. [001] oriented NWFETs for Ge, GaSb, and GeSn NWFETs exhibit the optimum balance, thus providing the highest I_{ON} among all orientations for the high

mobility materials. Also, with a carefully chosen value of S/D doping, they can outperform Si NWFETs despite having a higher SDT in OFF-state. Thus, they remain attractive alternatives to Si channel based p-MOSFETs at L_G=10 nm, unlike high mobility materials for n-channel FETs, which underperform compared to Si-based n-channel MOSFETs, for high performance logic devices. Hence for devices with a small gate length, where strain has limited effectiveness in improving device performance, the current study provides useful guidelines in the selection of materials and orientations, thereby providing a technological solution to minimize the impact of SDT in nanowire p-MOSFETs.

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