Finite element analysis of flip – chip on board (FCOB) assembly during reflow soldering process

Annapurna Addagarla and N. Siva Prasad
Department of Mechanical Engineering, Indian Institute of Technology Madras, Chennai, India

Abstract
Purpose – Out-of-plane displacement (warpage) is one of the major thermomechanical reliability concerns for board-level electronic packaging. The warpage and residual stresses can cause unreliability in the performance of electronic chip. An accurate estimation of the distortion and the residual stresses will help in selecting right combination of material for soldering and to determine the better assembly procedure of the chip. The purpose of this paper is to create a 3D nonlinear finite element model to predict the warpage, bending stresses, shear and peel stresses in a flip-chip on board (FCOB).
Design/methodology/approach – A 3D finite element procedure has been developed considering the material nonlinearity during solidification for a FCOB assembly. Finite element results have been compared with the experimental values.
Findings – The present finite element method gives better approximation of residual warpage and stresses compared to analytical models available in the literature.
Originality/value – The 3D finite element approach considering the elasto-plastic and temperature-dependent material properties has not been attempted by any authors. Experiments have been conducted for the comparison of finite element values. The finite element results compare better than the methods available in the literature. Hence a better method for estimating the deformation and residual stresses in flip-chip assembly has been suggested.

Keywords Soldering, Flow, Deformation, Stress (materials), Flip-chip, Reflow, Ball grid array, Residual stresses, Residual warpage

Paper type Research paper

1. Introduction

Flip-chip microelectronic assembly is the direct electrical connection of face down (flipped) electronic components onto substrates, circuit boards or carriers, by means of conductive bumps on the chip bond pads. Flip-chip, also called direct chip attach is composed of substrate (PCB), die (chip) and adhesive material (solder, a mixture of powder particles and flux). In the fabrication process of flip-chip, solder bumps are deposited on the metalized pads of the chip or die. The chip is face down (flipped) and position on the pads of the substrate. After fabrication, the whole die and substrate assembly undergoes a reflow soldering process consisting of four zones namely, preheat, preflow, reflow and cooling. In the first three zones, materials in the assembly are free to expand and solder bumps melt and flow. In the final zone, the assembly is cooled down from the peak temperature (above the melting point temperature of the solder) to the room temperature, the solder material get solidify and make permanent bond between the chip and substrate. Due to the difference between the coefficient of thermal expansion (CTE) between die and substrate, residual stresses and deformations are developed in the assembly.

Zhang *et al.* (2004) used finite element method (FEM) to model temperature distribution in a flip-chip no-flow underfill package during solder reflow process. They have considered the geometry of the flip-chip package and the thermal events including the phase transition of the solder material and exothermic underfill curing reaction. Brown *et al.* (1999) evaluated structural and thermal performance of a large, 10×10 mm, GaAs die, flip-chip attached to 25.4×25.4 mm diamond substrate using numerical, analytical and experimental methods. They have calculated stresses induced in die using temperature dependent, bi-linear solder plasticity properties. Liang *et al.* (2006) developed a finite element (FE) model for simulating reflow profile of solder balls in a forced convective airflow reflow furnace (impinging jet air flow furnace). Lee (1998) developed a FE model and described the structural instability of a PCB and its boundary conditions. Fu *et al.* (2002) examined the transient thermo-mechanical response of an unfilled plated through hole in an orthotropic double-layered printed wiring board assembly subjected to a typical wave soldering operation. Timoshenko (1925) examined mechanical behavior of bimetal thermostat based on elementary beam theory. Suhir (1989, 1996) developed models to predict shear stress and peel stress at the interface between two different materials based on Timoshenko's bimetal thermostat theory. Tsai *et al.* (2004) closely examined Suhir's method and suggested corrections to the solution and verified with the FE results. Park *et al.* (2004) developed a predictive model for the out of plane deformation for chip scale package (CSP) and chip on board (COB) assembly under temperature change using the classical lamination theory, and emphasized the importance of applying appropriate effective moduli using micro-mechanics model. Zhang *et al.* (2004) explained nonlinear FE analysis for solder joints. Vujosevic (2008) proposed an analytical solution for warpage of FCBGA and provided a tool for estimating the level and nature of influence of different material, geometric and processing parameters.

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In the present work, a 3D nonlinear FE model has been created using Ansys for the flip-chip assembly considering the melting of solder bumps and flow of solder material around the region of solder bumps and make permanent bond between the chip and substrate during cooling. A transient thermomechanical sequentially coupled field analysis was carried out to get the stress distribution and deformation in the die-substrate assembly. Temperature dependent material properties are used in the FE analysis. In thermal analysis the phase changes have been incorporated as a change in the specific heat of the solder material (Sn63-Pb37) in the melting range of temperature (183-184°C) and in structural analysis temperature dependent bi-linear plasticity properties with tangent modulus of 0.1 times Young's modulus (by iterations) were considered for calculating deformation and stress. These values are validated with the Tsai *et al.* (2004) closed form solution and experimental values.

2. FE analysis

2.1 FE model

A three dimensional FE model using Ansys has been developed for a flip-chip on board (FCOB) assembly shown in Figure 1. One fourth of the model is considered for the analysis making use of the symmetry. Lead-tin based solder material Sn63-Pb37 is considered as bonding material in the form of 10×10 ball grid array (BGA) with a ball (solder bump) size of 1.5 mm, and pitch 2 mm. The shape of the solder bump is sphere with top and bottom flat for stability at the start of the assembly process. Solder bumps are placed on the aluminum pads of size 1.5 mm and thickness of about 0.5 μm, for bonding the silicon die and solder balls. These aluminum pads are not considered in FE model as they do not contribute for carrying load because of negligible thickness. Residual stress and deformation are calculated in two steps:

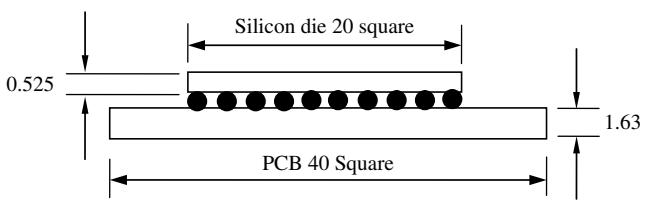
1 heat flow or thermal analysis; and
2 structural analysis.

(i) Thermal analysis

The first step in computation of residual stresses and distortions is the estimation of temperature profiles due to the forced convection in the reflow furnace. Eight-node hexahedron elements (SOLID70) applicable for steady-state and transient thermal analysis. The number of elements in the assembly is 176,400. Materials and their temperature dependent thermal properties are shown in Table I. Latent heat of Sn63-Pb37 solder 45.4 kJ/kg is incorporated as specific heat within the melting range (melting point temperature of Sn63-Pb37 solder is 183°C) shown in Figure 2.

During heating, material is free to expand and flow, and the temperature is uniform at the end of reflow. But during cooling process, distortions and residual stresses are developed, due to non-uniform temperature over the solder area. Hence, only cooling process is considered in the present work. The flip-chip assembly is cooled from the peak temperature of the reflow processes (230°C) to the room temperature (30°C). Insulating boundary conditions are applied at the surfaces of symmetry and forced convective coefficient of 26 W/m^2K (Liang *et al.*, 2006) is applied to the surfaces exposed to the furnace.

Figure 1 Flip-chip assembly



Note: Dimensions in "mm"

(ii) Structural analysis

The same FE model is used for both thermal and structural analysis. The 3D elements (SOLID70) used for thermal analysis are replaced by equivalent structural elements (SOLID45), having x, y and z translational degrees of freedom at each node. The temperature dependent mechanical properties (Table II) and bi-linear plasticity properties with tangent modulus of 0.1 times Young's modulus (by iterations) were taken into account for calculating the stress distribution. FE model with symmetric displacement boundary conditions with displacement $z = 0$ at the origin is shown in Figure 3. Temperature loads obtained from the thermal analysis are applied in the structural analysis.

3. Analytical model

The relationship between bending moment and curvature in pure bending of plates from Timoshenko and Woinowsky-Krieger (1956) is:

$$M_x = D'\left(\frac{1}{r_x} + \nu\frac{1}{r_y}\right) = -D'\left(\frac{\partial^2 w}{\partial x^2} + \nu\frac{\partial^2 w}{\partial y^2}\right) \quad (1)$$

$$M_y = D'\left(\frac{1}{r_y} + \nu\frac{1}{r_x}\right) = -D'\left(\frac{\partial^2 w}{\partial y^2} + \nu\frac{\partial^2 w}{\partial x^2}\right) \quad (2)$$

where:

$$D' = \frac{Et^3}{12(1-\nu^2)} \quad (3)$$

If bending moments $M_x = M_y = M$, spherical bending of plate is assumed, and the flexural rigidity of spherical bending of plate is:

$$D = \frac{Et^3}{12(1-\nu)} \quad (4)$$

A schematic diagram of FCOB assembly and free body diagram under thermal loading are shown in Figures 4 and 5, respectively. The assumptions of Tsai *et al.* (2004) are used made for calculating the stresses and warpage.

3.1 Warpage of CSP assembly

CSP is defined as package whose chip-to-package area ratio is greater than 80 percent. As per Tsai *et al.* (2004), solution curvature of the assembly in *x*-direction is:

$$K_x = \frac{1}{\rho(x)} = \frac{t\Delta\alpha\Delta T}{2\lambda D}\left(1 - \frac{\cosh\ kx}{\cosh\ kl}\right) \quad (5)$$

Warpage of assembly along the *x*-axis can be obtained by integrating the curvature equation (5):

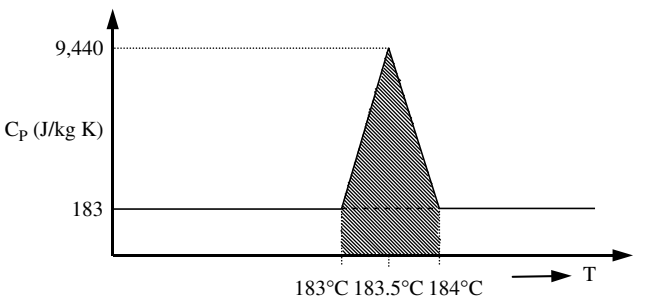
$$w(x) = \frac{t\Delta\alpha\Delta T}{2\lambda D}\left[\frac{1}{2}x^2 - \frac{\cosh\ kx - 1}{k^2\cosh\ kl}\right] \quad (6)$$

Table I Materials and their thermal properties

	Density (kg/m^3)	Thermal conductivity k (W/m K)		Specific heat C_p (J/kg K)	
FR-4 substrate	220	0.2		840	
Sn63-Pb37 solder	851	53		183	
Silicon die		*Temp °C*	*k*	*Temp °C*	C_p
	2,329	27	156	27	713
		127	105	127	785
		227	80	227	832
		327	64	327	849

Source: Fu *et al.* (2002) and Zhang *et al.* (2004)

Figure 2 Specific heat capacitance of Sn63-Pb37 solders including phase transition



Flexural rigidity of BGA can be written as (Harvey, 1974):

$$D = \frac{EI}{d} \tag{7}$$

where d is the pitch of the BGA and I is the area moment of inertia of the ball grid.

The warpage of the substrate in the die shadow region shown in Figure 6 are of the spherical bending type and the out of plane displacement at point C (Figure 6) can be written as:

$$w_C = w(x_C, y_C) = \frac{M}{2D(1+\nu^2)}x_C^2 + \frac{M}{2D(1+\nu^2)}y_C^2$$
$$= \frac{M}{2D(1+\nu^2)}x_A^2 + \frac{M}{2D(1+\nu^2)}y_B^2 = w_A + w_B \tag{8}$$

Table II Materials and their mechanical properties

	Young's modulus Mpa	Poison's ratio ν	Coefficient of thermal expansion α, 10^{-6}/°C
FR-4 substrate	22.4	0.143	26
Sn63-Pb37 solder	75.8-0.15 × T	0.35	24.7
Silicon die	130	0.278	2.60

Notes: *T* is absolute temperature in K
Source: Fu *et al.* (2002) and Zhang *et al.* (2004)

Figure 3 FE model with structural boundary conditions

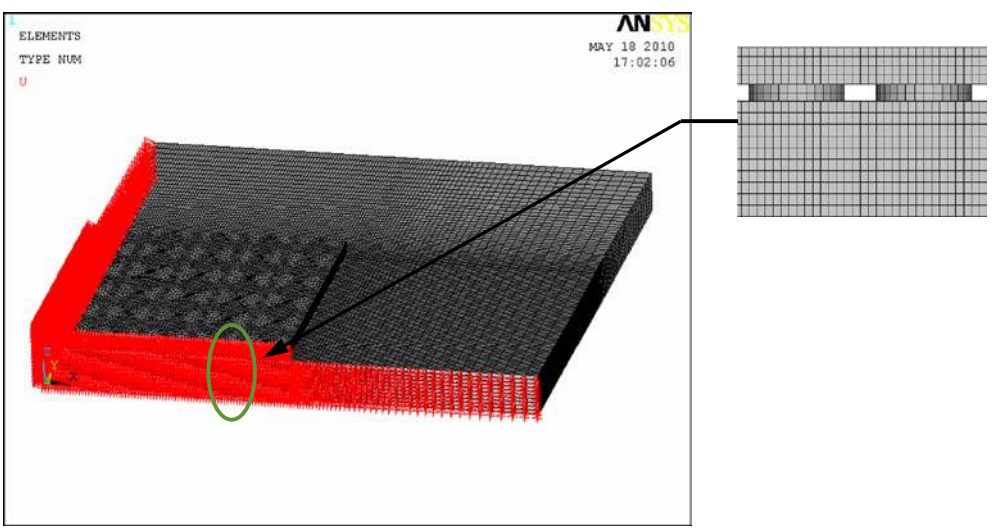


Figure 4 Geometrical and material parameters of a CSP

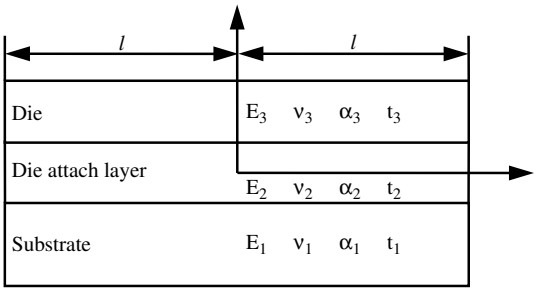


Figure 5 Free body diagram under thermal loading

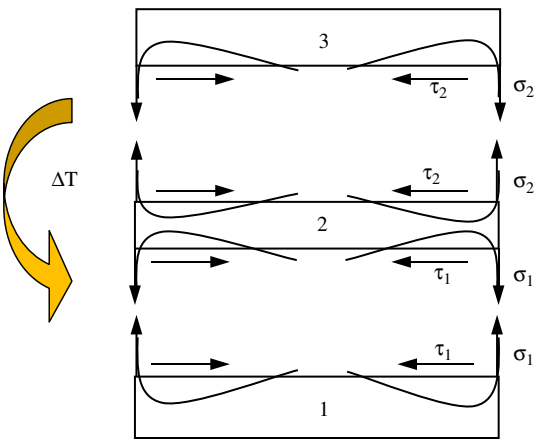
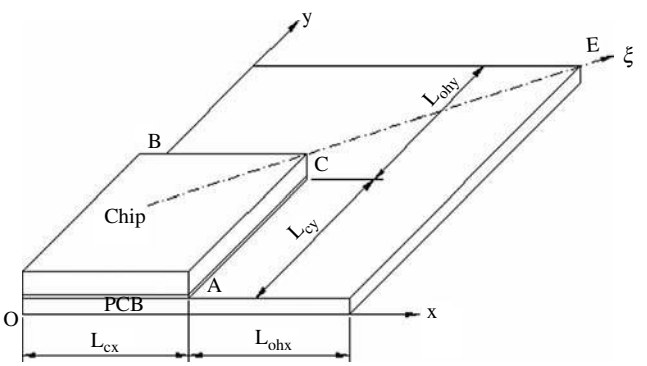


Figure 6 Die substrate assembly with overhang PCB (COB assembly)



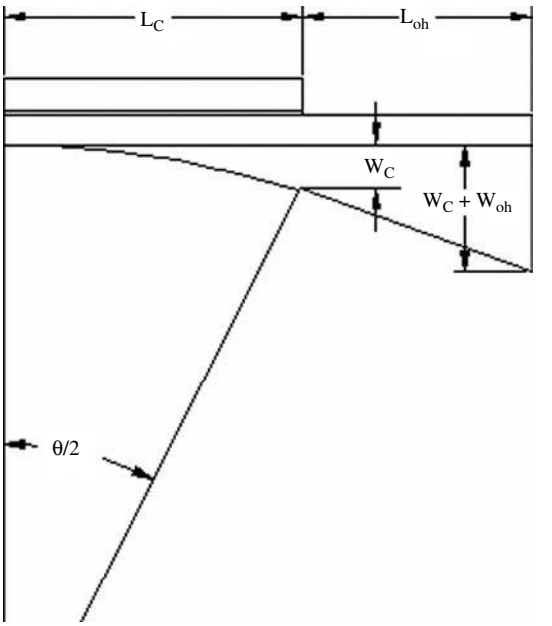
Transverse displacement of point C is equal to the sum of displacements of points A and B (Figure 6); for the square die these displacements are identical ($x_C = x_A = y_C = y_B$ and $w_A = w_B$) and therefore $w_C = 2w_A$, i.e.:

$$w\left(L_{cx}\sqrt{2}\right) = 2w(L_{cx}) \tag{9}$$

3.2 Warpage of COB assembly

In the previous section, the length of the substrate beyond the chip was ignored. To consider the overhang of the substrate beyond the edge of the chip, a three-layered structure depicting a flip-chip package with a larger substrate is shown in Figure 6. A line diagram of the warpage with overhang is shown in Figure 7. Half length of the substrate is:

Figure 7 Warpage of chip package with overhang



$$L = L_{cx} + L_{ohx} \tag{10}$$

Out of plane deformations at chip edge along *x*- and *y*-axis for the model can be calculated using equation (6), whereas, the out of plane deformation of overhang along the *x*- and *y*-axis can be approximated (Park *et al.*, 2004) as:

$$w_{ohx} = L_{cx}L_{ohx}K_x \tag{11}$$

$$w_{ohy} = L_{cy}L_{ohy}K_y \tag{12}$$

$$w_x = w_{cx} + w_{ohx} \tag{13}$$

$$w_y = w_{cy} + w_{ohy} \tag{14}$$

Assuming the continuity of slope at point C (Figure 6), and the slope outside the die region is constant, slope of the overhang substrate for the square die assembly can be written as:

$$\left.\frac{dw}{dx}\right|_{x=x_A} = L_{cx}K_x \tag{15}$$

The displacement along the diagonal, C-E, for $\xi \geq L_{cx}\sqrt{2}$ is (Vujosevic, 2008):

$$w(\xi) = \Delta\alpha\Delta T\frac{t}{2\lambda}\left(L_{Cx} - \frac{2}{k^2} + \frac{2}{k^2\cosh(kL_{Cx})} + \left(L_{Cx} - \frac{tgh(kL_{Cx})}{k}\right)\left(\xi - L_{Cx}\sqrt{2}\right)\right) \tag{16}$$

Peak warpage (maximum out of plane displacement) obtained at $w_{max} = w_E$.

3.3 Die attach shear stress

The die attach shear stress (τ_0) can be written as (Tsai *et al.*, 2004):

$$\tau_0 = \frac{k\Delta\alpha\Delta T}{k\ \cosh\ kl}\sinh\ kx \tag{17}$$

3.4 Die attach peel stress

As per (Tsai *et al.*, 2004) the die attach peel stress can be written as:

$$\sigma_0(x) = \frac{\mu\Delta\alpha\Delta T}{K}\ \frac{s^4}{1+s^4}\left[\frac{\cosh\ kx}{\cosh\ kl} + A_0V_0(\beta x) + A_2V_2(\beta x)\right] \tag{18}$$

3.5 Stresses distribution in die along *x*-direction

The die stresses in the longitudinal direction can be written as (Tsai *et al.*, 2004):

- Along the top line:

$$\sigma_{Top} = \frac{\Delta\alpha\Delta T}{\lambda t_3}\left(1 - 3\frac{tD_3}{t_3D}\right)\left(1 - \frac{\cosh\ kx}{\cosh\ kl}\right) \tag{19}$$

- Along the bottom line:

$$\sigma_{Bottom} = \frac{\Delta\alpha\Delta T}{\lambda t_3}\left(1 + 3\frac{tD_3}{t_3D}\right)\left(1 - \frac{\cosh\ kx}{\cosh\ kl}\right) \tag{20}$$

3.6 Stresses distribution in substrate along *x*-direction

The substrate stresses in the longitudinal directional direction can be written as (Tsai *et al.*, 2004):

- Along the top line:

$$\sigma_{Top} = \frac{\Delta\alpha\Delta T}{\lambda t_1}\left(1 - 3\frac{tD_1}{t_1D}\right)\left(1 - \frac{\cosh\ kx}{\cosh\ kl}\right) \tag{21}$$

- Along the bottom line:

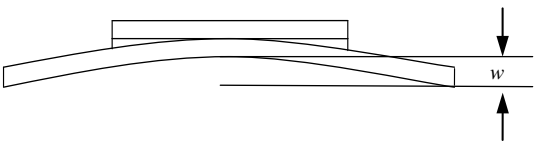
$$\sigma_{Bottom} = \frac{\Delta\alpha\Delta T}{\lambda t_1}\left(1 + 3\frac{tD_1}{t_1D}\right)\left(1 - \frac{\cosh\ kx}{\cosh\ kl}\right) \tag{22}$$

4. Experiments

To investigate the warpage of the FCOB assembly experimentally, a $20\,\text{mm} \times 20\,\text{mm} \times 525\,\mu\text{m}$ silicon die bumped with a full array of 100 Sn63-Pb37 solder bumps of diameter 1.5 mm with a pitch 2 mm and standoff height $250\,\mu$m is considered. Aluminum (Al) was metalized on silicon die in the form of 10×10 array. Nickel-phosphorus layer is plated on Al pads where solder bumps were fabricated subsequently. The solder bumps are dipped into flux and then aligned to the substrate using flip-chip bonder. After die attachment, the assembly has undergone through different zones of the reflow furnace which has nitrogen atmosphere. Last zone of the reflow furnace is cooling zone, where solder got solidified and made permanent bond between the die and the substrate.

The warpage in the cooled FCOB assemblies were measured to examine bending as a result of cooling of solder using co-ordinate measuring machine (Figure 8) having one micron accuracy. A total of twenty samples were prepared for the measurement of warpage and average values are taken for comparison. Care was taken not to allow any tilt of the assembly by proper alignment. Vertical displacement of the assembly is defined as the difference in elevation between center and edge.

Figure 8 Co-ordinate measuring machine (CMM) with FCOB



5. Results and discussion

Warpage in the flip-chip assembly is a result of the thermal stresses developed at the material interfaces due to the solidification of solder material during cooling process. The major cause of warpage in flip-chip assembly is difference in CTE between the silicon die 2.6×10^{-6}/°C and FR-4 substrate 26×10^{-6}/°C. While cooling the flip-chip assembly, the substrate contracts more than the silicon die and bends into a convex shape causing a "frowning face" warpage in the assembly as shown in Figure 9. A three dimensional FE model was created for calculating the stresses and deformations. The first step in the analysis is the estimation of temperature. Temperature profile for Sn63-Pb37 solder material is shown in Figure 10. Effect of phase transition on temperature of solder ball is evident as shown by small time step (~7 sec) at phase transition point 183°C, indicating latent heat release in the cooling process. Distortion and residual stress distribution are obtained in the structural analysis. Results obtained from the structural analysis are verified with analytical solutions available in the literature. Die and substrate are square plates, the assembly is subjected to uniform cooling and spherical bending of plates are assumed for analytical calculations. The warpage of the assembly, die attach shear, peel stress, die stress and substrate stress are calculated using equations (16)-(21).

A comparison of warpage between FEA, analytical and experiments on the *x*-*z* plane of symmetry is shown in Figure 11. The variations in warpage with reference to experimental values are shown in Table III. Variation in analytical values is large compared to FEA results. This may due to analytical solutions are derived within elastic region, whereas in the FEA, the solder material is considered as elasto-plastic. Figure 12 shows a comparision of shear stress distribution in the die attach layer (Sn63-Pb37 solder) along *x*-axis at *x*-*z* plane of symmetry between the FEA and analytical results. In the FE model die attach layer is in the form of BGA, the shear stress distribution along the center line of the bump at PCB side is varying as a wave form whereas it is smooth in the analytical method. This may be due to the discontinuity in the die attach material. There is a marginal variation in the maximum shear stress values between the FEM and maximum shear stress obtained from the analytical solution. Shear stress is zero at the center of the bump in FEA.

Figure 13 shows peel stress distribution in die attach layer along *x*-axis at *x*-*z* plane of symmetry between the FEA and analytical values. Peel stress distribution is also a wave form similar to shear stresses because of the discontinuity in the die attach layer. There is a variation of about 11 percent in maximum peel stress between the FEA and the analytical method. Stresses in solder balls inside area are tensile in nature, while solder balls at edge area are compressive in nature. Figures 14 and 15 show bending stresses in die and substrate along the top and bottom lines in *x*-axis direction. In the FEA the stresses in the die along the bottom is in wave form with mean line almost equal to analytical values. Along top line, the

Figure 9 Measurement of warpage in the flip-chip assembly

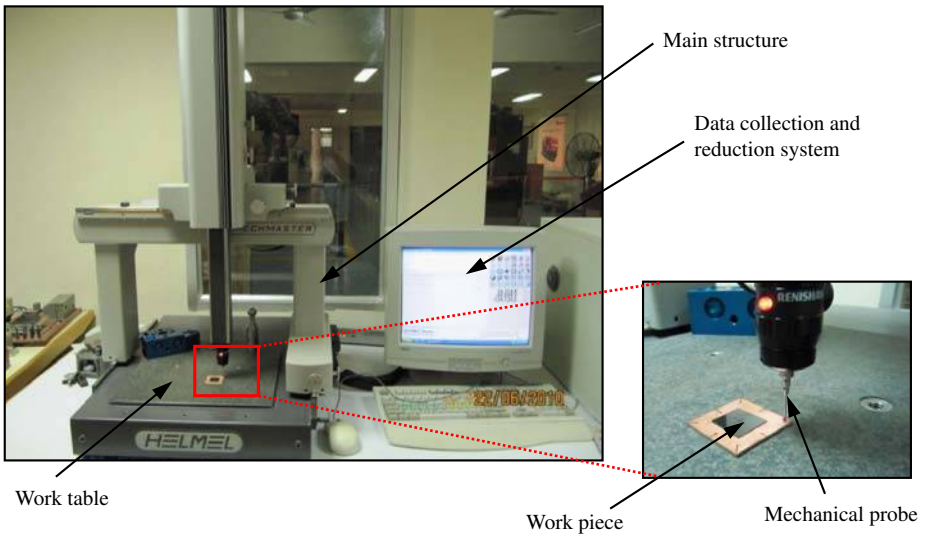


Figure 10 Temperature profile considering phase transition of solder material in cooling process

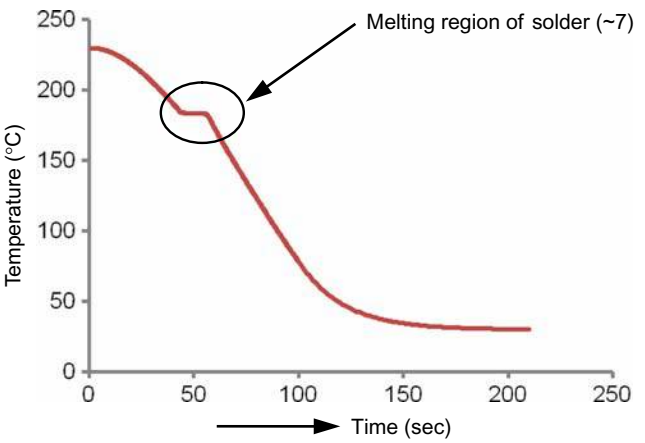
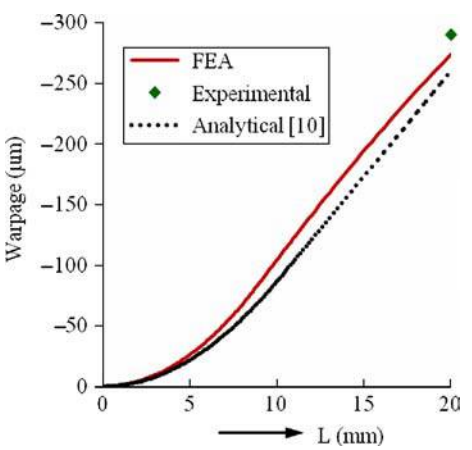


Figure 11 Warpage (deflection in *z*-direction) of the assembly on the *x-z* plane of symmetry



stresses are less at center of the die in FEA compared to analytical values. Variation in the PCB stress distribution along the top and bottom line in FEA is more compared to the analytical values because of the node at the origin was fixed in order to prevent rigid body displacement in FEA. Figure 16 shows warpage of the flip-chip assembly is spherical bending similar to the analytical method. Figure 17 shows von Mises stresses in the flip-chip assembly. The maximum stress is in the silicon die (187 MPa) and in the region of the bumps. Figure 18 shows principal stresses in the flip-chip assembly with a maximum values of 193 MPa in the silicon. von Mises stresses are used in the design PCB, solder bumps as they are ductile materials and principal stresses used for silicon as the material is brittle in nature.

6. Conclusion

In the present work, a 3D nonlinear FE model has been created to predict the warpage, bending stresses, shear and peel stresses in a FCOB. Nonlinear temperature dependent thermal and mechanical properties and phase transition effect of the solder material are considered in the FEA. The following conclusions are drawn:

- Warpage obtained in FEA is close to experimental values compared to analytical results. This may due to the analytical equations are derived within elastic region, whereas nonlinear temperature dependent mechanical and thermal properties beyond elastic region of solder material are considered in FEA.
- The stress distribution in the flip-chip is non-uniform and reaching maximum values near the bumps, whereas the analytical solutions give uniform stresses. This variation is because of the consideration of geometric irregularities due to the bumps and nonlinear temperature dependent properties of solder material during solidification.

Hence, the present method is more realistic for estimating residual warpage and stresses compared to the methods available in the literature.

Table III Comparision of warpage

	Experiments (μm)	FEA (μm)	Analytical (Park *et al.*, 2004) (μm)	% error FEA	% error Analytical (Park *et al.*, 2004)
Warpage at *x-z* plane of symmetry	−289	−274	−260	5.43	12.34
Peak warpage	−464	−442	−409	4.85	11.95

Figure 12 Shear stresses in the die attach layer (Sn63-Pb37 solder) at *x-z* plane of symmetry along *x*-axis

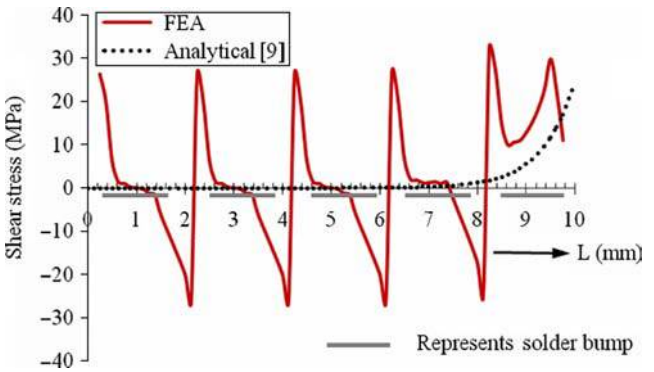


Figure 13 Die attach (Sn63-Pb37 solder) peel stresses at *x-z* plane of symmetry at PCB side along *x*-axis

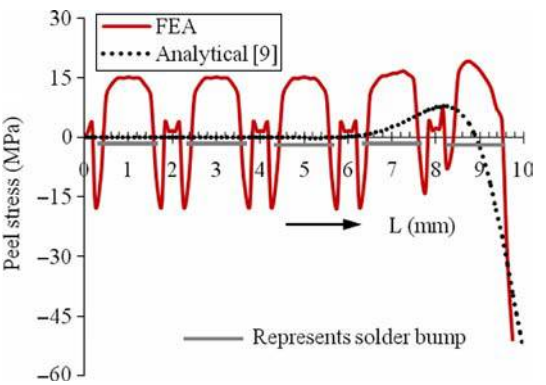


Figure 14 Bending stresses along top and bottom lines of the die in *x*-axis direction

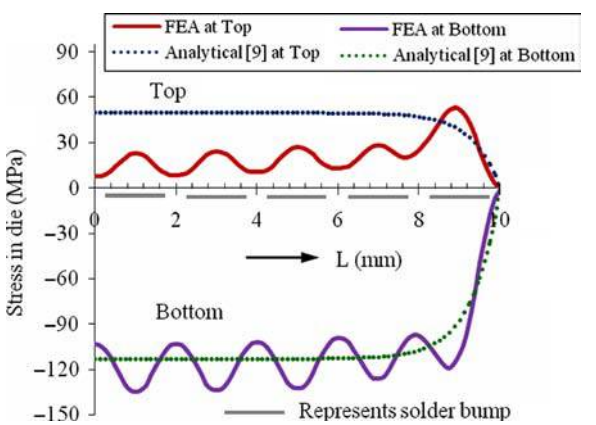


Figure 15 Bending stresses in substrate along top and bottom lines in *x*-axis direction

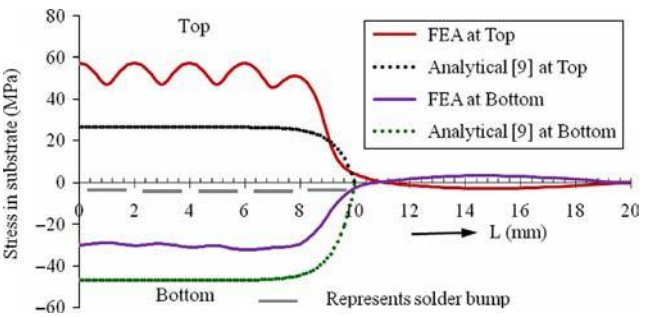


Figure 16 Warpage of flip-chip assembly (mm)

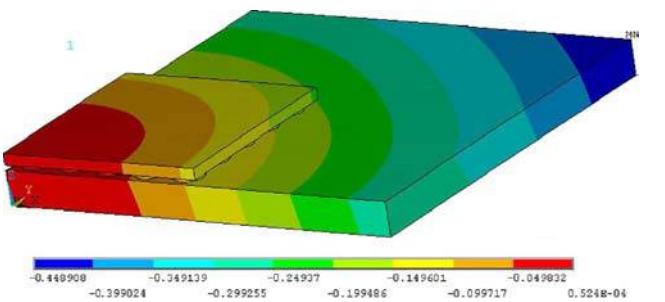


Figure 17 von Mises stresses in flip-chip assembly (MPa)

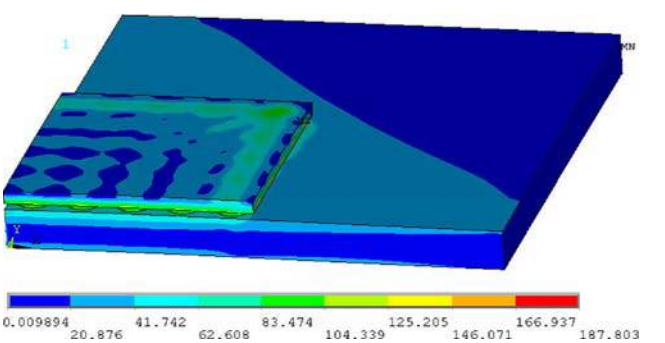
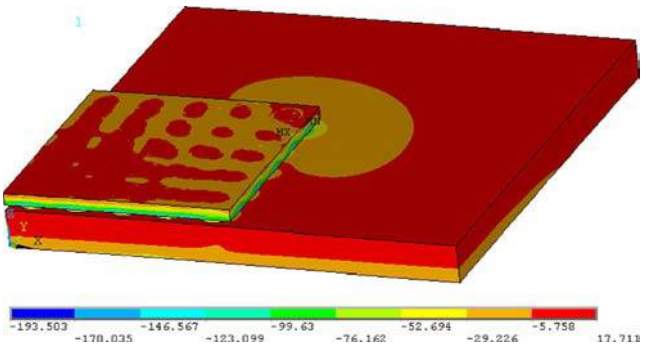


Figure 18 Principal stresses in the flip-chip assembly (MPa)



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Further reading

Li, Y. (2006), "Accurate predictions of flip-chip BGA warpage", *Report Altera*.

Corresponding author

N. Siva Prasad can be contacted at: siva@iitm.ac.in