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Electrical characterization of electron beam evaporated indium tin oxide/indium phosphide junctions

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The electrical properties of Indium tin oxide(ITO)/*p*-indium phosphide (InP) junctions prepared at different temperatures by reactive electron beam evaporation technique have been studied. A maximum of 10.0% photo conversion efficiency under 100 mW cm^{-2} illumination (without front metal grid and antireflection coating) has been observed. Analyses of the results indicate an interfacial oxide layer consisting of indium oxide and indium orthophosphate and the ITO/*p*-InP junction correspond to the semiconductor-insulator-semiconductor SIS model. An attempt has been made to understand the nature of the interfacial layer.

I. INTRODUCTION

High efficiency, excellent radiation resistance, and ease of preparation have made indium tin oxide (ITO)/*p*-indium phosphide (InP) solar cells quite attractive for space applications. Although several modules have been prepared and tested in satellites, very little has been achieved in the understanding of the junction formation and transport mechanism. It may be interesting to note that, so far, these ITO/InP junctions have been produced by sputtering: ion beam, rf, and dc magnetron[1–3] and spray pyrolysis techniques;[4–6] both techniques produce process induced defects in the junction. In the sputtering technique, it is believed that exposure of InP surface to plasma (either deposition or otherwise) brings out phosphorous deficient surface forming a buried homojunction yielding good photo conversion efficiencies. It is found that the deposition of indium (tin) oxide is not necessary at all for photovoltaic action.[7] In the spray technique, the high process temperatures (>400 °C) involved may lead to surface nonstoichiometry (loss of phosphorous) and the contamination levels may induce defects at the interface. The results of spray pyrolytic junctions have been interpreted[5,6] on the basis of an interfacial insulating layer. The theme of the present work is to prepare ITO/InP junctions by a technique which does not introduce process induced defects.

In the present work, reactive electron beam evaporation technique is used for the preparation of ITO/InP junctions. The effect of substrate temperature on the electrical properties of the junctions has been reported. X-ray photoelectron spectroscopic (XPS) studies on these junctions have also been made; relevant results have been reported here and a detailed analysis will be reported on separately.

II. EXPERIMENTAL DETAILS

The *p*-InP wafers used in the present work are magnesium doped: (2–6)$\times 10^{16}$ cm^{-3}, single side polished, (100) oriented, and procured from M/s Crystacomm. A second sample with Zn doping 1×10^{18} cm^{-3} is also employed for junction preparation. Standard procedures are followed for cleaning the wafers. The back ohmic contacts are made by depositing Au/Zn/Au in vacuum and alloying at 350 °C for 4 min in nitrogen atmosphere. Subsequently, prior to indium tin oxide (ITO) film deposition, the front surface of the InP wafer is etched with H_2SO_4:H_2O_2:H_2O::5:1:1 solution at room temperature (28 °C). The ITO was deposited onto a preheated InP substrate by evaporating pressed pellets of In_2O_3:SnO_2:95:5 by wt % using a 3 kW electron gun under controlled conditions following a procedure optimized to produce good quality ITO films.[8] The substrate temperature is controlled to an accuracy of ±2 °C. Clean glass substrates are also kept along with the InP wafers to confirm the quality of ITO films; the films are about 70–80 nm in thickness as measured by the multiple beam interferometry technique. Neither front contacts nor additional antireflection coatings have been made on the junctions. The area of the junctions is about 0.02 cm^2.

The cells of ITO/*p*-InP are characterized by current-voltage (I-V) and capacitance-voltage (C-V) measurements. The I-V measurements have been made under dark and illuminated conditions using a Keithley current meter (model 485) and a precision volt meter (Hindustan Instruments, India, Model HIL 2665). An illumination of 100 mW cm^{-2} measured by a power meter has been produced by a GE ELH lamp. The C-V measurements at 100 kHz have been recorded using a EG&G lock-in amplifier (model 5210) interfaced with a personal computer. During measurements the temperature of the ITO/InP cell was maintained at 27 ±0.5 °C.

The ideality factor, n, and the reverse saturation current density, J_0, for these junctions are evaluated from $\ln J$ vs V plots obtained by a variable illumination technique to eliminate the series resistance effects, if any; these values are given in Tables I and II.

J_0 and n values are also obtained from the dark I-V characteristics for various temperatures (130–390 K) and these values are used in the Richardson plot to evaluate effective barrier height (ϕ_b) and effective Richardson constant (A^*_{ox}).

All the results reported here are reproducible and are accurate to ±2%; hence no specific identification is given to the samples.

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TABLE I. Photovoltaic properties of ITO/p-InP junctions prepared on substrates of 6×10^{16} cm^{-3}.

T_s[a] (°C)	V_{oc}[b] (V)	J_{sc}[c] (mA cm^{-2})	J_0[d] (nA cm^{-2})	n[e]	ff[f]	η[g] (%)	R_s[h] (Ω)
150	487	23.2	34.7	1.3	0.47	5.3	271
175	506	30.9	20.7	1.3	0.64	10.0	49
200	510	29.7	280	1.7	0.42	6.4	292
225	465	22.1	1460	1.8	0.40	4.1	323

[a]T_s-substrate temperature.
[b]V_{oc}-open circuit voltage.
[c]J_{sc}-short circuit current density.
[d]J_0-reverse saturation current density.
[e]n-diode ideality factor.
[f]ff-fill factor.
[g]η-efficiency.
[h]R_s-series resistance.

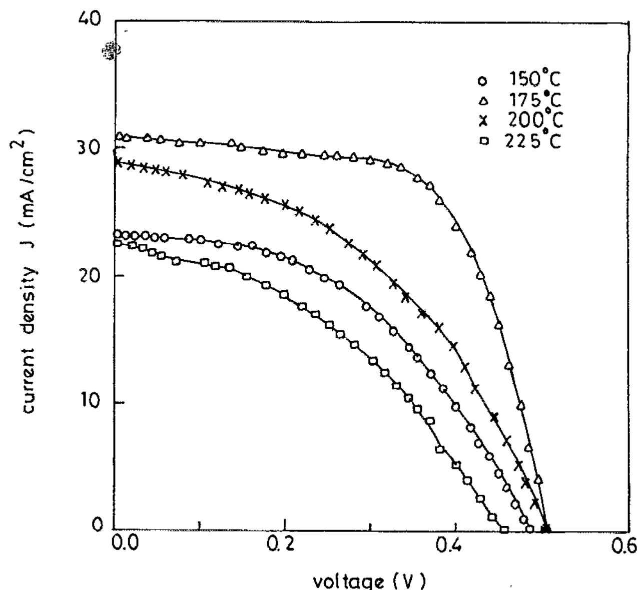

FIG. 1. Illumination I-V characteristics of ITO/p-InP junctions prepared at different substrate temperatures.

III. RESULTS

The present work, as mentioned earlier, is done on two InP substrates; unless otherwise specified, the data reported here correspond to the wafer having $(2-6)\times10^{16}$ cm^{-3} acceptor concentration.

A. Photovoltaic properties

Figure 1 shows the illuminated I-V characteristics of the junctions of ITO/p-InP prepared at different substrate temperatures in the range 150–225 °C. The photovoltaic parameters are listed in Table I. The open circuit voltage (V_{oc}) and the short-circuit current (J_{sc}) increase with substrate temperature up to 175 °C. The cells prepared at 175 °C exhibit a maximum efficiency of 10.0%, probably the highest value reported, so far, for electron beam evaporated ITO/InP junctions. The series resistance values of the cells have been calculated[9] and given in Table I.

It may be noted that in the present work, no front contacts have been used. In general for ITO/InP cells, the metal stack Cr/Pd/Au provides the front contact with low resistance conduction resulting in a high fill factor value thus enhancing the efficiency.

The spectral response curves for ITO/InP cells prepared at different substrate temperatures are shown in Fig. 2. The cells exhibit better short wavelength response than that of a homojunction cell.[10] Considerable reduction in short wavelength response is observed for cells prepared at higher substrate temperature (225 °C). All the curves exhibit a minimum around 500 nm, a feature not observed so far for ITO/InP junctions prepared by any other method. The sharp reduction in collection efficiency for these devices in the wavelength range 0.9–0.95 μm is due to the band edge of InP.

The photovoltaic parameters of the cells prepared on substrates with an acceptor concentration of 1×10^{18} cm^{-3} are listed in Table II. A maximum efficiency of 3.3% under 100 mW cm^{-2} has been achieved at a substrate temperature of 175 °C. Similar low efficiencies have been observed on

TABLE II. Photovoltaic properties of ITO/p-InP junctions prepared on substrates of 1×10^{18} cm^{-3}.

T_s[a] (°C)	V_{oc}[b] (V)	J_{sc}[c] (mA cm^{-2})	J_0[d] (nA cm^{-2})	n[e]	ff[f]	η[g] (%)	R_s[h] (Ω)
150	300	21.2	494	3.0	0.33	2.1	187
175	320	23.8	42	1.9	0.44	3.3	78
200	225	24.1	500	2.2	0.36	2.0	98
225	215	22.8	620	2.3	0.32	1.6	123

[a]T_s-substrate temperature.
[b]V_{oc}-open circuit voltage.
[c]J_{sc}-short circuit current density.
[d]J_0-reverse saturation current density.
[e]n-diode ideality factor.
[f]ff-fill factor.
[g]η-efficiency.
[h]R_s-series resistance.

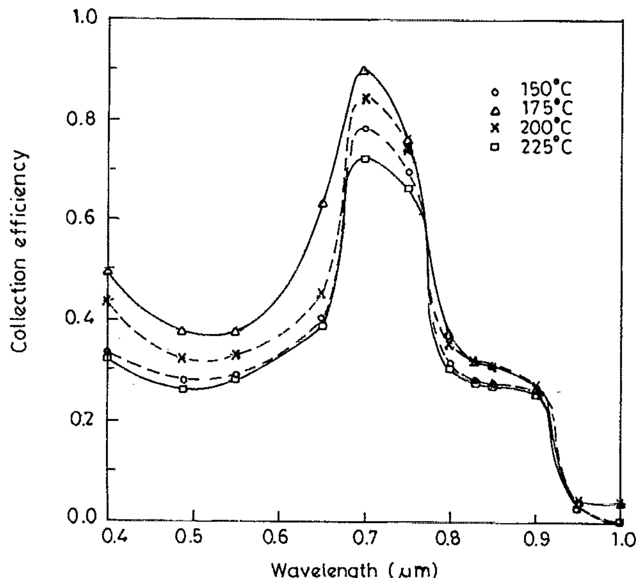

FIG. 2. Spectral response of ITO/p-InP junctions prepared at different substrate temperatures.

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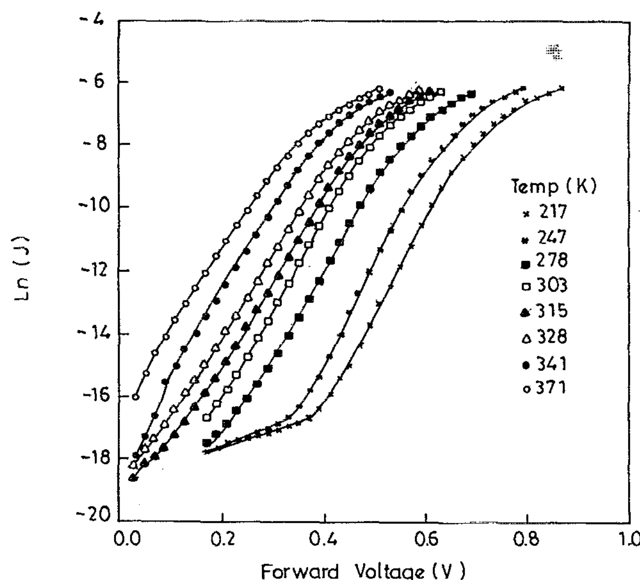

FIG. 3. Dark forward I-V characteristics of ITO/p-InP junctions prepared at 175 °C with temperature as a variable.

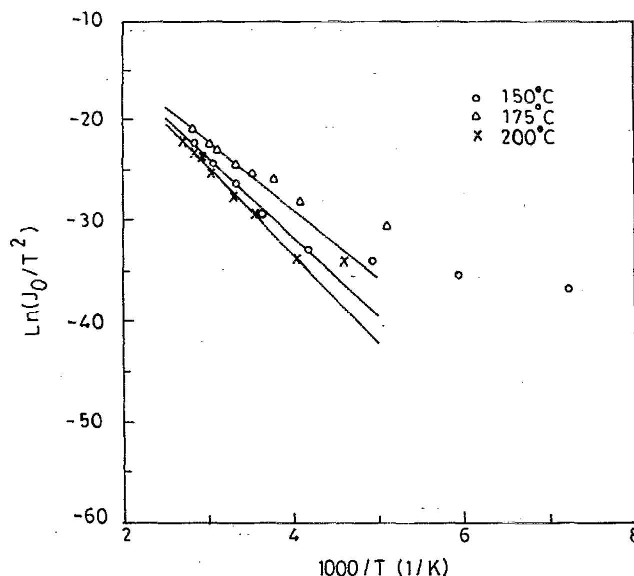

FIG. 4. Richardson plots for ITO/p-InP junctions prepared at different substrate temperatures.

heavily doped InP by earlier workers.[2] The efficiencies being quite low; no further analysis has been carried out on these samples.

B. Forward bias I-V properties

Figure 3 shows the forward bias plot of current versus voltage measured as a function of temperature in the range 217–371 K for an ITO/InP diode prepared at 175 °C.

At lower temperatures, the plots of $\ln J$ vs V (Fig. 3) have exhibited two slopes as has been commonly observed in the case of ITO/InP junctions prepared by other methods.[11,12] The diode ideality factor $n=1.3$ and >6 have been observed for higher and lower bias regions respectively.

The characterizing parameters of ITO/p-InP junctions prepared at different substrate temperatures are listed in Table III. The Richardson plot (Fig. 4), for a diode prepared at a substrate temperature of 175 °C gives an effective barrier height of 0.72 eV and the effective Richardson constant of $A^*_{ox} \approx 0.21\ \mathrm{A\,cm^{-2}\,K^{-2}}$.

TABLE III. Junction parameters of ITO/p-InP prepared on substrates of acceptor concentration 6×10^{16} cm^{-3}.

T_s (°C)[a]	$q\phi_b$ (eV)[b]	A^* (A cm^{-2} K^{-2})[c]	N_A (cm^{-3})[d]
150	0.72	0.68	1.3×10^{17}
175	0.72	0.21	4.2×10^{16}
200	0.56	0.009	2.4×10^{16}
225	...	...	2.2×10^{16}

[a] T_s-substrate temperature.
[b] ϕ_b-effective barrier height.
[c] A^*-effective Richardson constant.
[d] N_A-acceptor concentration.

C. C-V results

Figure 5 shows the $1/C^2$ vs V plots for ITO/p-InP junctions prepared at three different temperatures. The curves are linear in the entire bias range. The dopant concentration calculated from these plots agree with the value given. The built-in potentials observed from Fig. 5 are of the order of 2–3 V; similar unrealistic values have been reported earlier.[3,12] The C-V profiling carried out on these devices has been presented in Fig. 6.

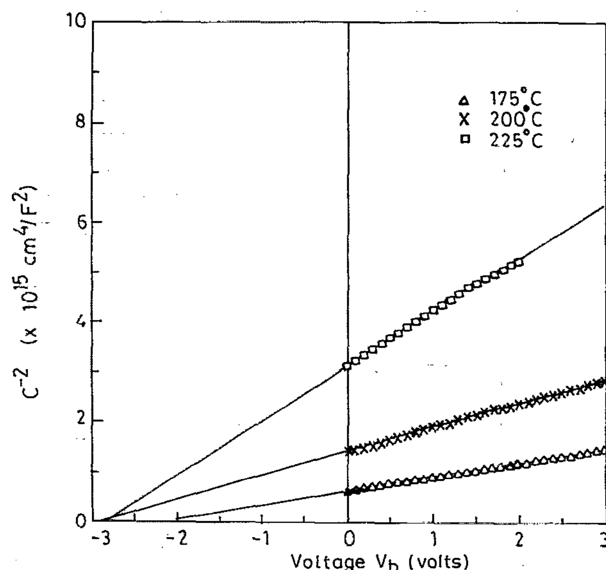

FIG. 5. $1/C^2$ vs V_b plot for ITO/p-InP junctions prepared at different substrate temperatures.

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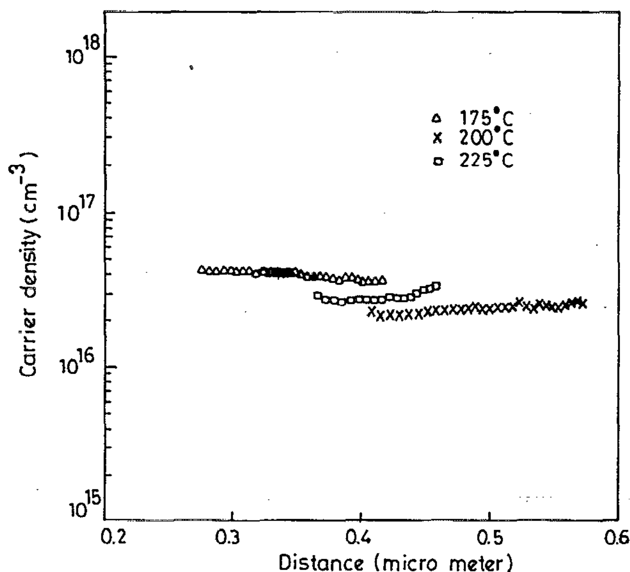
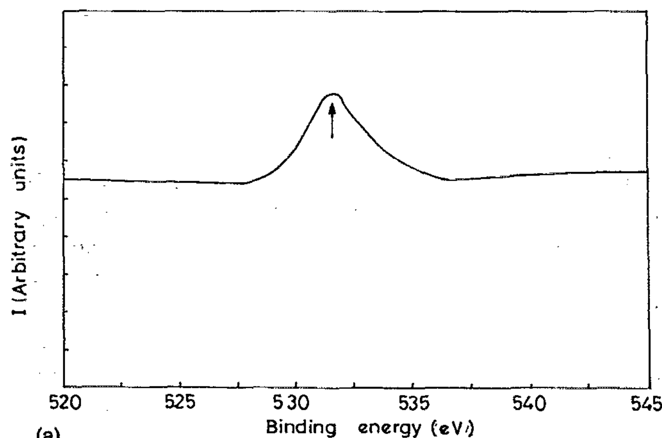


FIG. 6. Carrier concentration distribution for ITO/p-InP diodes.



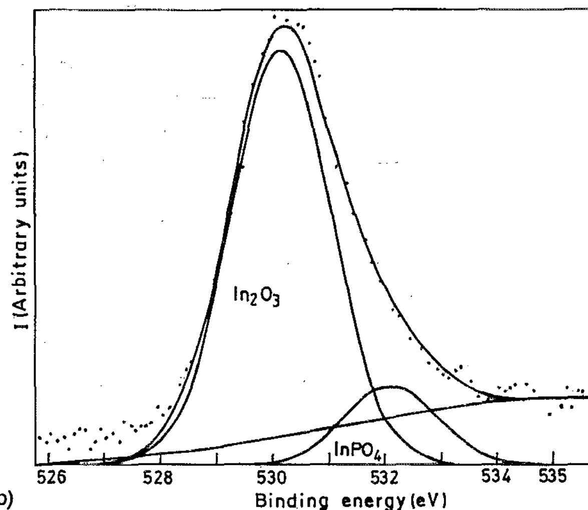


FIG. 7. (a) XPS O:1s spectra for p-InP surface after cleaning prior to ITO deposition. (b) XPS O:1s spectra for 5 min argon ion etch of thin ITO/p-InP (with 8 μA and 8 kV). Deconvoluted peaks correspond to In_2O_3, $InPO_4$, and linear background also is shown.

D. XPS results

Samples of as-cleaned InP wafers are examined by XPS (VG Scientific ESCALAB Mark II) using Mg K_α radiation. It showed signatures of indium (In:3d), phosphorus (P:2p), oxygen (O:1s) and carbon (C:1s contamination). The peak at a binding energy of 530 eV [Fig. 7(a)] corresponds to oxygen, which is present on InP just after cleaning indicating the presence of a thin native oxide on the surface of InP prior to ITO deposition.

A depth profile of XPS results (with argon ion etch at 8 μA for 5 min) at the interface of thin ITO(100 Å)/p-InP junction prepared at 175 °C reveal peaks corresponding to indium oxide (B.E=530.2 eV) and indium orthophosphate (B.E=532.1 eV) as shown in Fig. 7(b).[13]

IV. DISCUSSION

The salient observations of the present study may be summarized as follows:

(i) A maximum efficiency of 10.0% has been observed when the junctions are prepared at a substrate temperature of 175 °C.

(ii) With increase in substrate temperature above 175 °C (a) the efficiency of the cells decreases and (b) the reverse saturation current density J_0 increases.

(iii) The current-voltage characteristics measured for these junction (prepared at 175 °C) below 250 K exhibit two slopes demonstrating different transport mechanisms.

(iv) The built-in potentials calculated from the C-V plots have given anomalously large (unrealistic) values.

(v) XPS results show that there is a native oxide layer present on InP surface prior to ITO deposition.

(vi) Depth profile results of XPS on thin ITO/p-InP reveal interfacial oxides consisting of indium oxide and indium orthophosphate.

An understanding of these observations is possible provided the nature of the junction is known. The earlier results clearly demonstrated that high efficiency ITO/InP junctions are homoburied junctions[7] and the presence of donor like defects on p-InP has been observed in sputtered junctions.[12] The C-V profiling of the ITO/InP junctions in the present work (Fig. 6) has shown little evidence for n-type defects at the interface eliminating the possibility of homoburied junction.

With observations of extremely low Richardson constant ($A^*_{ox}=0.68-0.0087\times \mathrm{A\,cm^{-2}\,K^{-2}}$), signature of oxygen prior to ITO deposition and the presence of indium oxide and indium orthophosphate at the interface as shown by XPS results, a thin oxide layer at the interface is rather confirmed. The interfacial oxide layer plays a critical role in controlling the barrier height as well as the transport mechanism across the barrier. An attempt has been made to explain the observed results on the basis of semiconductor-insulator-semiconductor (SIS) model; the SIS model is similar to metal-insulator-semiconductor (MIS) structure because of the ITO window layer.

The current transport in MIS is given by

$$J_0=A^*_{ox}T^2\exp(-\phi_b/kT) \tag{1}$$

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and

$$A^*_{ox}=A^* \exp(-0.26\chi^{1/2}\delta),$$

where A^*_{ox} is the effective Richardson constant, ϕ_b is the barrier height, χ is the mean barrier height of the oxide-semiconductor interface, and δ is the interfacial oxide layer thickness. The barrier height from the present study ranges between 0.72–0.56 eV and the A^*_{ox} varies between 0.68 and 0.87×10^{-2} A cm^{-2} K^{-2}. The calculated barrier heights using theoretical A^* are in the range 0.75–0.86 eV; these values compare well with those reported recently.[14] It may be interesting to note that difference between ITO work function[15] and electron affinity of p-InP[16] gives the barrier height 0.99–1.14 eV. The thickness of the oxide layer has been calculated to be in the range 20–50 Å using $A^*=48$ A cm^{-2} K^{-217} and χ=0.5 eV.[12]

The improved performance of the ITO/p-InP SIS junction with substrate temperature indicates that the junction has optimum properties at 175 °C. The photoconversion efficiency of the junction formed at 200 °C is noteworthy as it yields high V_{oc} and J_{sc} in spite of the fact that it has large J_0 and R_s values. The large reverse saturation current density J_0 at $T_s=225$ °C diminishes the effective barrier height, as observed. The low fill factor results from relatively large series resistance values. At higher substrate temperatures the transport mechanism across the junction ($n=1.8$ at $T_s=225$ °C) deviates from the near thermionic emission ($n=1.3$) process.

The spectral response measurements (Fig. 2) of ITO/InP clearly indicate that the junctions are not of homo buried type (an increase in the quantum efficiency with decreasing photon energy till the band edge of InP is a characteristic feature of the homojunctions[10]). The junction prepared at 175 °C exhibits maximum short wavelength response corresponding to a shallow junction. The depth of the junctions from spectral response measurements do not match with the results of C-V profiling (Fig. 6).

The high built-in potential values and agreement of acceptor concentration from C-V plots of ITO/InP have also been observed by other workers and they have attributed the unrealistic barrier heights to complicating effects due to an insulating layer at the interface.[3] Attempts have been made to explain these high shifts in the bias axis by assuming an interfacial layer with and without fixed charges but with little success as also reported earlier.[18]

Concentrating our attention on the transport mechanism across the junction in these devices, it may be logical to assume that with increasing substrate temperature, either the interfacial oxide thickness or the nature of the oxide is expected to change. In either case the reverse saturation current J_0 should decrease, contrary to the observation. Further, increase in J_0 may be the reason for the reduction in the effective barrier height (from I-V). A calculation of the interface state density D_{its} from the observed ideality factor and the assumed oxide layer thickness

$$D_{its}=\epsilon_i(n-1)/q\delta. \quad (2)$$

It is observed that D_{its} is of the order of 10^{12} cm^{-2} eV^{-1}. D_{its} increases with substrate temperature deviating from the interfacial layer theory.[16] For the device prepared at 175 °C, the diode ideality factor n at high temperature, 371 K, is found to be 1.3 where as at lower temperature, 217 K (and higher bias) $n=1.7$. From these data one may infer that the thermionic-field emission process controls the current transport across the junction.[19]

The interfacial insulating layer may arise from the growth of native oxides of InP when exposed to high temperatures, particularly in oxygen ambients. Very little information is available on the energy structure of the native oxides of InP. For InP, the possible native oxides are In_2O_{3-x}, P_2O_{4-x}, and $InPO_{4-x}$, with χ value ranging from 0.2 to 1.2 eV.[20] Furthermore, the value may depend critically on the exact nature: stoichiometry, structure, etc. of the interfacial layer. The XPS data on the devices in the present work [Fig. 7(b)] confirms the presence of In_2O_3 and $InPO_4$ at the interface.

V. CONCLUSIONS

It has been shown that high efficiency ITO/p-InP cells can be made by using a reactive electron beam evaporation technique; a technique that does not introduce plasma induced defects. Present study gives a conclusive evidence that ITO/p-InP junctions are of SIS type and the interfacial insulating layer consists of indium oxide and indium orthophosphate.

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