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# Ambient field effects on the current-voltage characteristics of nanowire field effect transistors

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We investigate the effects of ambient field from the gate and drain contacts on the current-voltage characteristics of a vertical nanowire field effect transistor having a lightly doped ungated length near the drain. Such a device is suitable for high voltage (tens of volts) applications. It is shown that the ambient field enhances the carrier concentration and divides the ungated region into gate-controlled and drain-controlled sections, controllable by the drain contact size and bias-voltages. These phenomena have a significant impact on the drain breakdown voltage, saturation voltage, saturation current and output resistance. The effects are established with the help of measured data and numerically calculated current-voltage curves and field lines. © *2011 American Institute of Physics*. [doi:10.1063/1.3555426]

Nanowire (NW) devices have a high surface to volume ratio. Hence, their characteristics are governed not only by the field within the NW but also by the fringing or ambient field lines setup on the NW by potential variation on the NW surface and device contacts. The ambient field depends on the contact geometry. Literature has investigated the effect of ambient field on the current[1,2] in NWs and the capacitance[3] and conductance[4] of NW Schottky junctions. The present work reveals the effect of the ambient field on the *I-V* characteristics of certain NW metal oxide field effect transistors (NW MOSFETs).

NW MOSFETs have been projected[5] to provide integrated circuits with significantly better performance than planar MOSFETs. When fabricated in a vertical (V) configuration [see Fig. 1(a)], these devices have a high packing density, can be paralleled easily using a common top contact to increase the current levels, and do not face difficulties associated with handling and positioning of NWs horizontally as in pick and place approach. The fabrication process of a VNW MOSFET leaves an ungated NW length, $L_{DG}$, between the drain contact and the gate. The doping in $L_{DG}$ is the same as in the channel, and hence, light, unless additional processes such as ion implantation[6] or silicidation from metal contact[7] are employed to raise the doping or conductance in $L_{DG}$. The characteristics of a VNW MOSFET with lightly doped $L_{DG}$ have not been investigated, since the literature has been preoccupied with NW FETs for small-signal applications involving a few volts for which a lightly doped $L_{DG}$ plays an entirely parasitic role of introducing a drain resistance. Thus, NW MOSFET models available in literature invariably assume the $L_{DG}$ region to be heavily doped (e.g., Refs. 8 and 9) by some process.

However, to explore the potential of NW MOSFETs fully, one must also consider applications involving higher voltages (tens of volt), where conventionally, planar lightly doped drain (LDD) MOSFETs[10] have been employed. For such applications, like the LDD region of a planar MOSFET, the lightly doped $L_{DG}$ region of NW MOSFETs can spread and thus reduce the electric field, leading to higher breakdown voltage, improved hot electron reliability, and reduced short channel effects.[10] It is with this motivation that we investigate the current-voltage characteristics of a VNW MOSFET with a lightly doped $L_{DG}$. Of critical interest in this investigation is the effect of ambient field lines from the $L_{DG}$ region to the gate and drain contacts, since NW devices are sensitive to ambient field unlike the planar LDD MOSFETs. The drain contact of a VNW MOSFET extends by $L_E$ [see Fig. 1(a)] beyond the NW diameter unless this contact is the tip of a scanning tunneling microscope/atomic force microscope. Such a contact extension is also inherent in VNW MOSFETs connected in parallel by a common contact.

Our theoretical calculations and the measured data used to illustrate the ambient field effects correspond to a single device in a parallel combination of many VNW MOSFETs fabricated in Ref. 11. We choose this MOSFET because it has a lightly doped $L_{DG}$ and all its structural parameters are

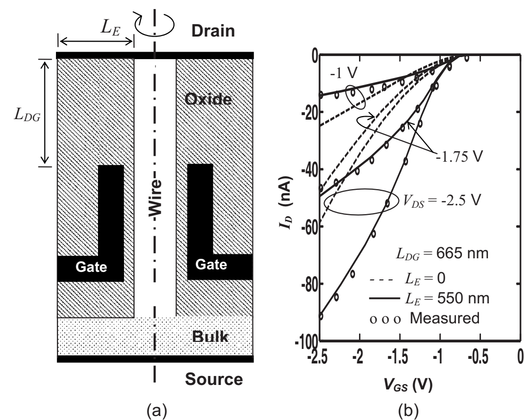


FIG. 1. (a) The cross-section of the silicon VNW-MOSFET considered in our work (diagram not to scale). Top contact is nickel-silicon Schottky, bulk contact is Ohmic, gate metal is chromium, substrate doping $=3\times10^{19}$ $cm^{-3}$ boron, NW doping $=3\times10^{16}$ $cm^{-3}$ boron, NW diameter $=25$ nm, gate oxide thickness $=35$ nm, gate length $=550$ nm. The drain contact extension $L_E=550$ nm and the ungated length $L_{DG}=665$ nm in Ref. 11. Our calculations also use values of $L_E=0$ and $L_{DG}=15,265$ nm. (b) Measured (circles) and calculated (lines) $I_D$-$V_{GS}$ curves. The measured current reported here is 131 times smaller than that in Ref. 11, since it corresponds to a single FET out of a parallel combination of 131 FETs fabricated and measured in Ref. 11.

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known. The outline of our work is as follows. First, we reveal the role of the ambient field from the drain contact in the measured $I_{DS}$-$V_{GS}$ (drain current versus gate-source voltage) data. Next, we calculate the ambient field picture and terminal characteristics up to breakdown by a simultaneous numerical solution of the transport, continuity and Poisson's equations;[12] the Poisson's equation is solved both inside and outside the NW to include the effect of the ambient field. The solution assumes the following models: transport in the NW is by drift-diffusion since the gate length is an order of magnitude higher than the ballistic limit;[13] band to band tunneling through Schottky contact is included. Quantum effects are neglected as NW radius >5 nm.[14] The gate electrode is equipotential. The perpendicular component of the flux is continuous across the NW/insulator interface (Ref. 11 suggests that interface charge for this device is negligible), and zero at the outer surfaces of the insulator implying that the fields from adjacent devices (in a parallel combination) do not overlap. Mobility degradation follows the equation $\mu = \mu_0[1+(E_\perp/E_c)+(\mu_0 E_\parallel/v_{sat})]^{-1}$, where $E_\parallel$, $E_\perp$ are parallel, perpendicular fields. Impact ionization follows the Van Overstraeten model which has been shown to predict the measured $V_{BR}$ of NW p-n junctions.[15] From these calculations, we establish that the $L_{DG}$ region can be partitioned into two parts $\alpha L_{DG}$ and $(1-\alpha)L_{DG}(0<\alpha<1)$ controlled by the ambient field from the drain and gate electrodes, respectively, where $\alpha$ depends on $L_E$ and the bias voltages; the $\alpha L_{DG}$ region spreads the electric field as the LDD of a planar MOSFET. Based on this phenomenon, we explain how, for large $L_E$, the drain breakdown voltage, $V_{Dbr}$, saturation voltage $V_{Dsat}$, saturation current, $I_{Dsat}$, and output resistance in saturation all are significantly higher than those for $L_E$=0, and the degradation of $I_{Dsat}$ with increase in $L_{DG}$ is arrested.

The experimental device of Ref. 11 consists of 131 P-channel VNW MOSFETs connected in parallel by a common drain contact. The structure and $I_{DS}$-$V_{GS}$ curves of Fig. 1 correspond to a single MOSFET in this parallel combination. The calculated curves (using SENTAURUS TCAD tool[16]), match the measured data as shown in Fig. 1(b) using $\mu_0$=6.89 cm$^2$ V$^{-1}$ s$^{-1}$, $E_C$=100 KV cm$^{-1}$ and $v_{sat}$=8.37 $\times 10^6$ cm s$^{-1}$. The low $\mu_0$ is close to the lower limit of 7.5 cm$^2$ V$^{-1}$ s$^{-1}$ extracted in Ref. 11 from transconductance measurements, and is attributed to excessive scattering from the NW surface beneath the gate. Next, we recalculate the $I_{DS}$-$V_{GS}$ curves by setting $L_E$=0 to suppress the ambient field from the drain contact. Figure 1(b) shows that the shape and magnitude of the curves with $L_E$=0 differ significantly from those curves for large $L_E$, and so, cannot be scaled to match the measured data by any parameter adjustment. This confirms the role of the ambient field from the drain contact.

The above phenomenon is clarified further by the ambient field and potential lines of Fig. 2(a), shown for $L_E$=0 and $L_E$=550 nm at two different values of $V_{DS}$=−1, –2.5 V and $V_{GS}$=−2.5 V<threshold voltage, $V_T$=−0.62 V. Potential over the ungated length $L_{DG}$ is greater than the drain potential, and for the $V_{GS}$ considered ($\leq V_{DS}$), greater than the gate potential as well. Hence, for $V_{DS}$=−1 V as well as $V_{DS}$=−2.5 V, the field lines connecting the $L_{DG}$ region to the gate and drain originate from $L_{DG}$, increasing the hole concentration and hence the conductivity of $L_{DG}$. For $V_{DS}$=−1 V, when $L_E$ is extended, the origin of many of these field lines near the drain shifts from the $L_{DG}$ to $L_E$,

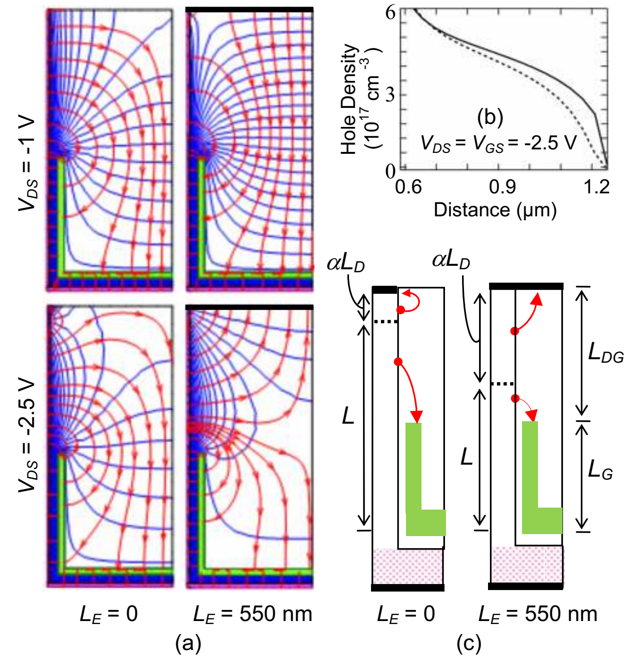


FIG. 2. (Color online) (a) Simulated potential lines and field vectors in the right-half of the device cross-section; $V_{DS}$=−1 V (top two), –2.5 V (bottom two); $L_E$=0 nm (left two), 550 nm (right two); $V_{GS}$=−2.5 V and $L_{DG}$ =665 nm. (b) Hole distribution along the NW axis over the ungated length $L_{DG}$=665 nm for $V_{DS}$=$V_{GS}$=−2.5 V. (c) Schematic illustrating the division of $L_{DG}$ into gate-controlled and drain-controlled portions, and the effective channel length $L$, for $L_E$=0 (left) and $L_E$=550 nm (right). Arrows (→) from $L_{DG}$ represent field lines.

reducing the hole accumulation and conductivity of $L_{DG}$. This explains why, in Fig. 1(b), $I_{DS}$ for $L_E$=550 nm is lower than that for $L_E$=0. The situation is reversed at $V_{DS}$=−2.5 V. In this case, as $L_E$ is extended, more and more field lines emanating from the NW near the drain prefer to terminate on the nearby $L_E$ rather than on the far away gate. Shorter field lines near the drain imply a higher field strength and so more hole accumulation there. Thus, for large $L_E$, more holes accumulate near the drain [see Fig. 2(b)] and result in higher $I_{DS}$ [see Fig. 1(b)]. Note from Fig. 2(b) that hole accumulation due to the ambient field would not have modulated the conductivity of the $L_{DG}$ region, if the NW doping were $>6\times 10^{17}$ cm$^{-3}$, i.e., heavy. However, such a heavily doped $L_{DG}$ cannot spread the electric field.

The ambient field pictures of Fig. 2(a) lead to the following model for $L_{DG}$ illustrated in Fig. 2(c). The ambient field lines from the $\alpha L_{DG}$ part of the ungated region terminate on the drain contact and those from the remaining $(1-\alpha)L_{DG}$ part terminate on the gate. Therefore, effectively, the device has a resistive length $\alpha L_{DG}$ which spreads the electric field in saturation, and a channel length $L=L_G+(1-\alpha)L_{DG}$. When either $V_{DS}$ or $L_E$ is increased, for a given $V_{GS}$, $\alpha$ increases and the effective channel edge is pushed toward the gate edge. For a device with $L_E$=0, the increase in $\alpha$ with $V_{DS}$ is small, i.e., the effective channel edge remains close to the drain contact implying $L\approx L_G+L_{DG}$, and only a small region is available for spreading the electric field. On the other hand, for large $L_E$, $\alpha$ increases with $V_{DS}$ and approaches unity as the $V_{DS}$ approaches $V_{Dsat}$, i.e., in saturation, the effective $L\approx L_G$ and the field can spread over the entire $L_{DG}$. This model is confirmed by locations of the calculated peak field [see Fig. 3(a)] near the drain contact for

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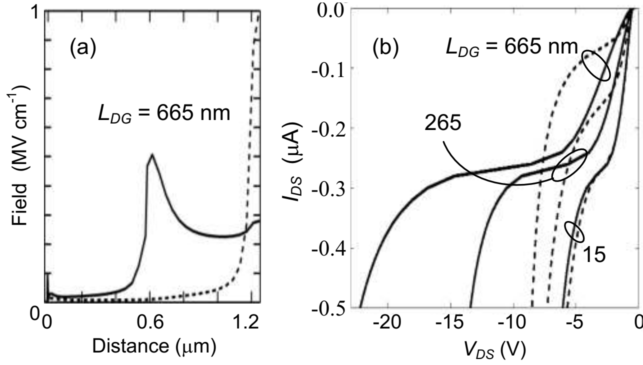


FIG. 3. (a) Field distributions at breakdown along the NW axis from source to drain. (b) $I_{DS}$-$V_{DS}$ curves showing the effect of $L_{DG}$ and $L_E$. In (a) and (b), $V_{GS}=-2.5$ V, and the dashed, solid lines are for $L_E=0,550$ nm.

$L_E=0$ and near the gate edge for large $L_E$ at breakdown (according to MOSFET theory,[10] the peak field at breakdown lies near the channel edge).

We provide a first order quantitative validation of the above model by demonstrating that the model's simple analytical predictions of $V_{Dbr}$, $I_{Dsat}$, $V_{Dsat}$, and output resistance, given below, roughly match the numerical calculations of Fig. 3(b).

(1) The model predicts that $V_{Dbr}$ increases with $L_{DG}$ as $V_{Dbr}=(-4-\alpha L_{DG}E_{br})$, where $E_{br}=0.3$ MV/cm and –4 V is the numerically calculated $V_{Dbr}$ for $L_{DG}=0$. For large $L_E$, $\alpha=1$ leads to a large increase in $V_{Dbr}$ with $L_{DG}$ as per $V_{Dbr}=-4.4$, –12, –24 V for $L_{DG}=15$, 265, 665 nm; when $L_E=0$, the values of $V_{Dbr}=-4.1$, –5.2, –7 V for $L_{DG}=15$, 265, 665 nm [see Fig. 3(b)], that imply much smaller increment in $V_{Dbr}$ with $L_{DG}$, are obtained using $\alpha=0.15$, which is indeed small in accordance with the model.

(2) The model predicts $I_{Dsat}\propto(V_{GS}-V_T)^2/L$, where $L=L_G+(1-\alpha)L_{DG}$. For large $L_E$, we have $\alpha=1$ yielding an $I_{Dsat}$ roughly independent of $L_{DG}$. In contrast, for $L_E=0$, we have $\alpha\ll 1$, so that $I_{Dsat}$ decreases as reciprocal of $L\approx L_G+L_{DG}$, in fact a little faster on account of a small increase in $V_T$ with increase in $L_{DG}$ due to weakening of the gate fringing field at the channel edge. Further, we have $[(I_{Dsat}$ for large $L_E)/(I_{Dsat}$ for $L_E=0)]>[(L_G+L_{DG})/L_G)]$, since ($V_T$ for $L_E=0$) $>$($V_T$ for large $L_E$) because, for $L_E=0$, the gate field which modulates the $L_{DG}$ portion of the channel is "fringing" type, and so, weaker than the field beneath the gate. Consequently, for $L_{DG}=665$ nm and $L_G=550$ nm, we get $[(I_{Dsat}$ for large $L_E)/(I_{Dsat}$ for $L_E=0)]>2.2$.

(3) The model predicts $V_{Dsat}\approx V_{GS}-V_T+V_O+I_{Dsat}R_D$, where $V_O$ is the voltage across Schottky drain contact, $(V_O-V_T)$ is small enough to be negligible for the device considered and $R_D=[1/(qp\mu)]\alpha L_{DG}/(\pi R^2)$ is the resistance of the $\alpha L_{DG}$ region. We may, therefore, write $V_{Dsat}\approx V_{GS}+[I_{Dsat}/(qp\mu\pi R^2)]\alpha L_{DG}$. For $L_E=0$, we have $\alpha\ll 1$ leading to $V_{Dsat}\approx V_{GS}=-2.5$ V roughly independent of $L_{DG}$ (the small decrease with $L_{DG}$ is due to $V_T$ variation with $L_{DG}$). However, for large $L_E$, we have $\alpha=1$ and $[I_{Dsat}/(qp\mu\pi R^2)]=3.6\times10^{-3}$ V nm$^{-1}$ using $p=6\times10^{17}$ cm$^{-3}$, $\mu=15$ cm$^2$/V s and $R=12.5$ nm, where $p>$ the average value in Fig. 2(b) since $|V_{Dsat}|>2.5$ V for which Fig. 2(b) is plotted, and $\mu>\mu_0$ since scattering beneath the gate which afflicts $\mu_0$ does not afflict $\mu$ over $\alpha L_{DG}$. Consequently, $V_{Dsat}$ increases as $V_{Dsat}=-2.5-3.6\times10^{-3}L_{DG}$ ($L_{DG}$ in nm)$=-2.6,-3.4,-4.9$ V for $L_{DG}=15$, 265, and 665 nm.

(4) The field spreads over $\alpha L_{DG}$ where $\alpha=0.15$ [calculated in (1)] for small $L_E$ and $\alpha=1$ for large $L_E$. Since the field spreads over a longer length for large $L_E$, the theory of planar LDD MOSFET (Ref. 10) predicts that channel length modulation in saturation is much less, or the output resistance is much more, for large $L_E$ than that for $L_E=0$.

In conclusion, we established the following effects of the ambient field from the gate and drain electrodes in VNW MOSFETs having lightly doped ungated length near the drain. The ambient field enhances the carrier concentration in the ungated length and divides this length into gate and drain controlled sections, controllable by the drain contact extension and bias voltages. For large drain contact extension, drain breakdown and saturation parameters are much higher than those for no drain contact extension, and the degradation of saturation current with increase in ungated length is arrested. Consequences of these results on design, parameter extraction, and modeling of NW devices will be dealt with in a separate work.

[1]H. Ruda and A. Shik, J. Appl. Phys. **84**, 5867 (1998).
[2]A. A. Talin, F. Leonard, B. S. Swartzentruber, X. Wang, and S. D. Hersee, Phys. Rev. Lett. **101**, 076802 (2008).
[3]A. Achoyan, S. Petrosyan, W. Craig, H. E. Ruda, and A. Shik, J. Appl. Phys. **101**, 104308 (2007).
[4]J. Hu, Y. Liu, C. Z. Ning, R. Dutton, and S.-M. Kang, Appl. Phys. Lett. **92**, 083503 (2008).
[5]R. Yerushalmi, Z. A. Jacobson, J. C. Ho, Z. Fan, and A. Javey, Appl. Phys. Lett. **91**, 203104 (2007).
[6]B. Yang, K. D. Buddharaju, S. H. G. Teo, N. Singh, G. Q. Lo, and D. L. Kwong, IEEE Electron Device Lett. **29**, 791 (2008).
[7]W. M. Weber, L. Geelhaar, A. P. Graham, E. Unger, G. S. Duesberg, M. Liebau, W. Pamler, C. Che'ze, H. Riechert, P. Lugli, and F. Kreupl, Nano Lett. **6**, 2660 (2006).
[8]J. Yang, J. He, F. Liu, L. Zhang, F. Liu, X. Zhang, and M. Chan, IEEE Trans. Electron Devices **55**, 2898 (2008).
[9]B. Yu, W. Y. Lu, H. Lu, and Y. Taur, IEEE Trans. Electron Devices **54**, 492 (2007).
[10]S. Ogura, P. J. Tsang, W. W. Walker, D. L. Critchlow, and J. F. Shepard, IEEE J. Solid-State Circuits **15**, 424 (1980).
[11]J. Goldberger, A. I. Hochbaum, R. Fan, and P. Yang, Nano Lett. **6**, 973 (2006).
[12]S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices* (Wiley, New York, 2007).
[13]K. H. Cho, K. H. Yeo, Y. Y. Yeoh, S. D. Suk, M. Li, J. M. Lee, M.-S. Kim, D.-W. Kim, D. Park, B. H. Hong, Y. C. Jung, and S. W. Hwang, Appl. Phys. Lett. **92**, 052102 (2008).
[14]S.-H. Oh, D. Monroe, and J. M. Hergenrother, IEEE Electron Device Lett. **21**, 445 (2000).
[15]P. Agarwal, M. N. Vijayaraghavan, F. Neuilly, E. Hijzen, and G. A. M. Hurkx, Nano Lett. **7**, 896 (2007).
[16]Sentaurus Device User Guide, version C, Synopsys, 2009.

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