

# A Two-Dimensional Numerical Simulation of Oxide Charge Buildup in MOS Transistors Due to Radiation

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**Abstract**—We have developed a time-dependent two-dimensional simulator in order to simulate charge trapping in silicon dioxide due to radiation. The Poisson and continuity equations are solved both in the oxide and the semiconductor. In addition, in order to simulate charge trapping, trap rate equations using first-order trapping kinetics are solved in the oxide. This paper contains the numerical methods used in the simulation and results obtained using this simulator. One of the main results of this simulation is the presence of a lateral variation in the radiation-induced oxide charge in an MOS transistor irradiated with a drain bias.

## I. INTRODUCTION

ONE of the important total dose effects in metal-oxide-semiconductor (MOS) transistors is the buildup of positive charge in silicon dioxide which leads to long-term threshold voltage shifts. This charge buildup occurs due to the trapping of radiation-generated holes in deep traps near the interface. The amount of charge trapped is very sensitive to the bias conditions during irradiation and very often, a nonuniform charge develops in the gate oxide across the channel. This in turn affects the behavior of the MOS transistor. In order to understand the behavior of the MOS transistor after irradiation, this oxide charge must be known accurately. This is possible only if the Poisson and continuity equations are solved both in the oxide and the semiconductor, along with the trap rate equations in the oxide. In previous simulations [1]–[3], the effect of radiation induced oxide charge is taken into account by assuming a laterally uniform charge at the interface. This is insufficient as the drain current is sensitive to the variations in the oxide charge. We have developed a complete two-dimensional time-dependent simulator in order to find the oxide charge under various bias conditions. The effect of this radiation-induced charge on the operation of the MOS transistor is studied. This paper contains the numerical methods used in our simulator and the results obtained using this simulator.

## II. EQUATIONS AND BOUNDARY CONDITIONS

In order to obtain the trapped charge, the following equations need to be solved. In the oxide,

$$\nabla^2 \psi = -\frac{q}{\epsilon_{\text{ox}}}(p + p_t - n - n_t)$$

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$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot J_p + G_{\text{ox}} - \sigma_p v_{\text{th}} p (N_{\text{tp}} - p_t) + e_p p_t$$

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n + G_{\text{ox}} - \sigma_n v_{\text{th}} n (N_{\text{tn}} - n_t) + e_n n_t - \sigma_r v_{\text{th}} n p_t$$

$$\frac{dp_t}{dt} = \sigma_p v_{\text{th}} p (N_{\text{tp}} - p_t) - e_p p_t - \sigma_r v_{\text{th}} n p_t$$

$$\frac{dn_t}{dt} = \sigma_n v_{\text{th}} n (N_{\text{tn}} - n_t) - e_n n_t$$

and in the semiconductor,

$$\nabla^2 \psi = -\frac{q}{\epsilon_{\text{si}}}(D + p - n)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot J_p$$

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n$$

In the above equations,

$$J_p = q p \mu_p E - q D_p \nabla p$$

$$J_n = q n \mu_n E + q D_n \nabla n$$

are the electron and hole currents represented by the drift-diffusion model both in the oxide and the semiconductor. One-dimensional simulations show that it is sufficient to use the drift-diffusion model for both electron and hole currents in order to get the flatband voltage shifts at room temperature [4], even though it is known that holes move dispersively in SiO<sub>2</sub>. The electron and hole mobilities in the oxide are taken to be 20 cm<sup>2</sup>/V-s and 10<sup>-5</sup> cm<sup>2</sup>/V-s respectively [5].

$\psi$ ,  $n$ ,  $p$ ,  $p_t$  and  $n_t$  are the electrostatic potential, electron and hole densities and the trapped hole and electron densities, respectively.  $N_{\text{tp}}$  and  $N_{\text{tn}}$  are the hole and electron trap densities in the oxide. Experimentally it has been found that the hole traps are situated within 50–100 Å of the interface, with a peak trap density between 10<sup>18</sup>–10<sup>19</sup>/cm<sup>3</sup> for dry oxides [5]. We have assumed a gaussian distribution of hole traps, with a peak value between 10<sup>18</sup>–10<sup>19</sup>/cm<sup>3</sup> and the centroid within 50–100 Å of the interface. The width of the gaussian distribution is taken to be between 50 Å and 100 Å. The exact values used are mentioned for each of the simulations performed. The hole trap density is assumed to be uniform in the lateral direction. Experiments show that electron traps are uniformly distributed with the trap density for dry oxides being about 10<sup>17</sup>/cm<sup>3</sup>, which is the value used in the simulations. Although the electron trap density is only an order of magnitude lower than the hole trap density, electron trapping does not usually result in any significant degradation

due to the large mobility of electrons.  $\sigma_p$  and  $\sigma_n$  are hole and electron capture cross-sections for capture by neutral traps which typically have a value of  $10^{-18}$  cm<sup>2</sup>. The hole capture cross-section is reported to have a much higher value in the literature and this discrepancy is discussed in greater detail in a previous paper [6].  $\sigma_r$  is the capture cross-section for recombination of electrons with trapped holes and is taken to be  $10^{-15}$  cm<sup>2</sup>, which is approximately the capture cross-section for capture of electrons by coulombic attractive traps. The measured value of the thermal activation energy of the hole traps is between 0.7–1.4 eV [5]. In our simulations, this energy variation has been neglected and both hole and electron traps are assumed to have an activation energy of 0.7 eV. This results in emission probabilities due to thermal detrapping of trapped holes and electrons,  $e_p$  and  $e_n$ , of about  $10^{-4}$ /s. It is to be noted that since we are interested only in the trapping characteristics, a different value for the emission time will merely change the saturation value of the threshold voltage shift. Its variation with dose, electric field etc. will not be affected. Also, detrapping by tunneling to silicon is neglected.

$G_{ox}$  is the generation rate of electron-hole pairs in the oxide which is obtained from the experimental value of the dose rate. Generation and recombination of carriers are neglected in the semiconductor. Although this will not give the correct carrier concentration in the semiconductor during irradiation, it will not affect the trapped charge in the oxide significantly since there is negligible injection of carriers from silicon into the oxide due to the large barrier height.

Depending on whether the transistor is *n*- or *p*-channel, only the electron or hole continuity equation is solved in the semiconductor, but all the equations are solved in the oxide. This is reasonable as there is no significant hole current in an *n*-channel transistor and vice versa except for very short channel devices. Therefore, this model reduces essentially to a heterojunction with SiO<sub>2</sub> modelled as a wide band gap semiconductor. One-dimensional simulations show that this is a fairly accurate model [6]. The vacuum level is used to represent the electrostatic potential and the equilibrium fermi level is used as the reference.

The structure used is a typical MOS structure as shown in Fig. 1, with field oxide included between the gate oxide and the source and drain contacts. The source, drain and substrate contacts are assumed to be ohmic contacts. At the gate contact CD also, ohmic boundary conditions were used. The gate contact is clearly not an ohmic contact, but this boundary condition can be used since we have neglected the thermionic injection current [7]. Along the artificial boundaries AB, EF, and the field oxide boundaries, it was assumed that the normal component of the current and the electric field is zero. At the Si-SiO<sub>2</sub> interface, Gauss's law was used directly. Current continuity and continuity of the quasi-fermi level [7] are assumed to be the interface conditions for the continuity equations. The former condition arises because we have assumed that there are no oxide traps at the interface. The interface states that are present can be assumed to charge up instantaneously in response to the effective gate bias (including the shift due to the bulk oxide charge). Once again the thermionic injection current across the interface is neglected.

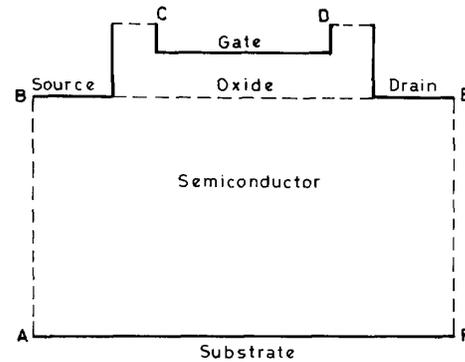


Fig. 1. The MOS transistor structure used in the simulations.

The gate boundary conditions and the interface conditions imply that the carrier concentrations are not accurate close to the two interfaces. Therefore the trapped charge within 20–30 Å of the two interfaces is less than expected. (Our simulations show that quasi fermi level falls steeply within 20–30 Å of the interface.) But this will not create much of an error in the total trapped charge, since most of the deep hole traps are further away than 20 Å from the Si-SiO<sub>2</sub> interface, and the trapped charge within 20–30 Å of this interface is in practice annealed out by electrons tunneling into the oxide from silicon [5].

The MINIMOS 4.0 mobility model was used for carrier mobilities in silicon [8]. This model includes mobility variation with doping density, surface scattering, gate field and velocity saturation. Radiation-induced mobility degradation has not been included, since most of this degradation arises due to the buildup of interface states, which has not been included because there is no well accepted physical model for interface-state generation in a radiation environment. However, the effect of interface states on the *I*-*V* characteristics can be simulated if the interface state distribution with energy is specified.

### III. METHOD OF SOLUTION

The grid as well as the initial guess is obtained using the solution of the one-dimensional Poisson equation and the charge sheet model for the MOS transistor [9]. The spatial discretization was done using the finite difference method with the Scharfetter-Gummel scheme used for the continuity equations and the time discretization using the second order Gear's method. Nonuniform time steps were obtained depending on the local truncation error [10]. The coupled Newton method was used to solve the discretized nonlinear equations.

Both direct (sparse LU decomposition with a dynamic minimum degree ordering [11]) and iterative methods (based on the conjugate gradient algorithm) were tried out for the linear solvers. Since the Jacobian of the Poisson equation is symmetric and positive definite, the conjugate gradient method with an incomplete Cholesky preconditioner (ICCG) was used [12]. Since the Jacobian of the coupled equations does not have any special properties, the conjugate gradient squared method (CGS) method was used [13]. Both incomplete LU

(ILU) and a block incomplete LU (BILU) decompositions [14] were tried out as preconditioners. In addition, we have tried out the LU-GCR method [15] which has been previously used only in circuit simulation [16]. In this method, an LU decomposition is done for the steady state solution (or for the solutions at any particular time step). For all other Newton iterations, the generalized conjugate residual (GCR) method is used, with the most recent LU as the preconditioner. We have used it to solve the steady state equations, doing a complete LU until the error in the Newton iteration (measured relative to the value of the unknown) reduces to less than 0.1. In the subsequent Newton iterations, GCR was used with the last LU as the preconditioner and it typically converged in less than 5 iterations. This method is especially useful in cases where the initial guess is not very good, in which case initially the direct method performs better than the iterative methods and later on as the solution is approached it is preferable to use iterative methods. Since GCR performs very well with an LU preconditioner, this method is able to combine the advantages of both.

As mentioned previously, radiation incident on a biased device often results in a spatially nonuniform charge across the channel. Therefore, in order to calculate the threshold voltage ( $V_T$ ), simple analytic models based on a one-dimensional electric field cannot be used and at least a two-dimensional Poisson equation must be solved. In order to obtain the threshold voltage shift as a function of the dose, typically the threshold voltage calculation has to be done several times during a simulation, which makes it unfeasible to solve the entire coupled set of equations to find the threshold. Instead, we have solved the one-dimensional continuity equation along with the two-dimensional Poisson equation using the Gummel's method. This gives a value of  $V_T$  that is within 0.03 V of the value obtained using a full two-dimensional simulation and is very fast. In all our simulations a constant current threshold definition was used, i.e. the threshold voltage is taken to be the gate voltage at which the normalized drain current  $I_D/(W/L)$ , is  $10^{-7}$  A at an applied drain voltage of 0.25 V.

#### IV. RESULTS OF THE SIMULATION

In the steady state the simulator was tested against MINIMOS 4.0. Fig. 2 shows a typical comparison of the output characteristics for an  $n$ -channel device from MINIMOS and our simulator (RADMOS). A comparison with MINIMOS of the subthreshold characteristics is shown in Fig. 3. There is still a slight difference in the two currents, and this is because we have not been able to get the exact values of the material parameters used in MINIMOS.

Figs. 4 and 5 show the threshold voltage shifts obtained for a transistor irradiated under zero drain bias and different gate biases. Also shown in this figure are the flatband voltage shift with time obtained using a one-dimensional simulator and published experimental data [17], [18]. Assuming no interface traps are generated, a good correlation is expected between the flatband shifts in an MOS capacitor and the threshold voltage shifts in an MOS transistor irradiated under zero drain bias. The comparison with experimental data is made

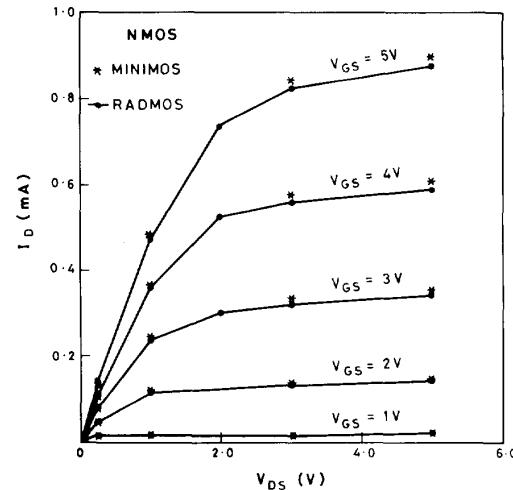


Fig. 2. A comparison of the output characteristics obtained from MINIMOS 4.0 (\*) and our simulator RADMOS (●) for an  $n$ -channel device ( $L_{EFF} = 3 \mu\text{m}$ ). The data obtained using our simulator have been connected by straight lines for ease of visualization.

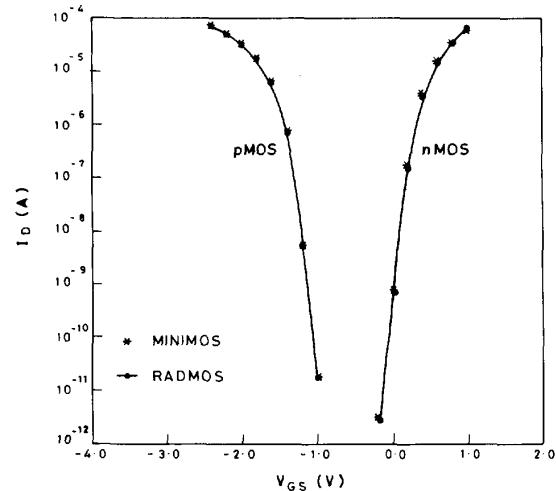


Fig. 3. A comparison of the subthreshold characteristics obtained from MINIMOS 4.0 (\*) and our simulator RADMOS (●) for a  $p$ -channel device ( $L_{EFF} = 1.5 \mu\text{m}$ ) and  $n$ -channel device ( $L_{EFF} = 4 \mu\text{m}$ ).

by keeping all parameters fixed and varying only the peak value of the trap density until a reasonable comparison is obtained. From the figures, it is seen that the simulator is able to predict the shape of the curve very well. It is seen that the threshold shifts in the transistor (two-dimensional simulation) correlates well with the flatband shifts in the capacitor (one-dimensional simulation), the correlation being better at lower doses and higher values of the applied electric field. This is understandable since the two situations are similar until the field due to the trapped charge begins to dominate.

Fig. 6 shows the flatband voltage shift at different points in the channel for  $n$ -channel transistors irradiated in the triode ( $V_{GS} = 2 \text{ V}$ ,  $V_{DS} = 1 \text{ V}$ ) and saturation ( $V_{GS} = 2 \text{ V}$ ,  $V_{DS} = 5 \text{ V}$ ) regions. This flatband shift is calculated by finding the

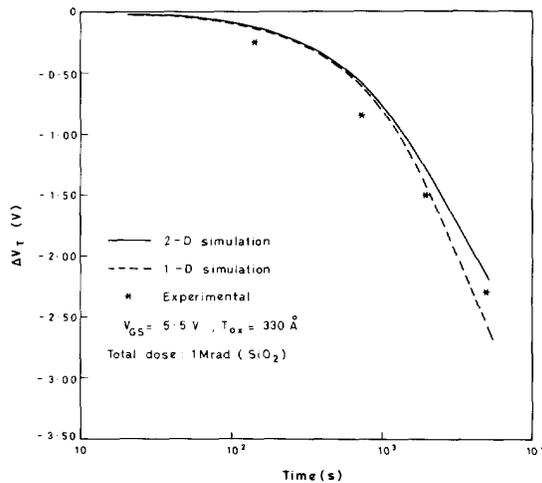


Fig. 4. A comparison of the threshold voltage shift in an MOS transistor (two-dimensional simulation) with the flatband voltage shift in an MOS capacitor (one-dimensional simulation) and with published experimental data [17]. The peak trap density used is  $10^{18}/\text{cm}^3$ , the width of the gaussian distribution is 60 Å and the location of the centroid is at 50 Å from the interface. The oxide thickness is 330 Å. The values of the capture cross sections are mentioned in the text.

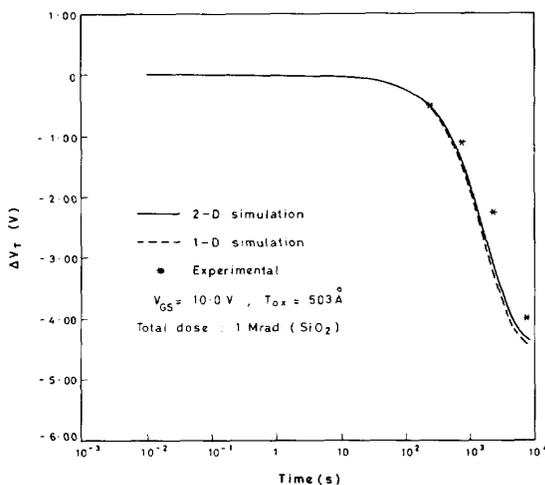


Fig. 5. A comparison of the threshold voltage shift in an MOS transistor (two-dimensional simulation) with the flatband voltage shift in an MOS capacitor (one dimensional simulation) and with published experimental data [18]. The peak trap density is  $10^{18}/\text{cm}^3$ , the width of the gaussian distribution is 60 Å and the location of the centroid is at 53 Å. The oxide thickness is 503 Å. The values of the capture cross-sections are mentioned in the text.

centroid of the trapped charge along each vertical grid line. If irradiated in the triode region it is seen that the charge near the drain end of the channel is slightly larger than at the source end. This is understandable because, beyond a certain positive voltage, the flatband shift decreases slightly with an increasing oxide electric field [6] (essentially due to a decrease in the capture efficiency of the traps). As the electric field at the source end of the channel is larger, it contains a slightly smaller amount of positive charge. Normally, it is the energy barrier at the source that determines the threshold voltage and

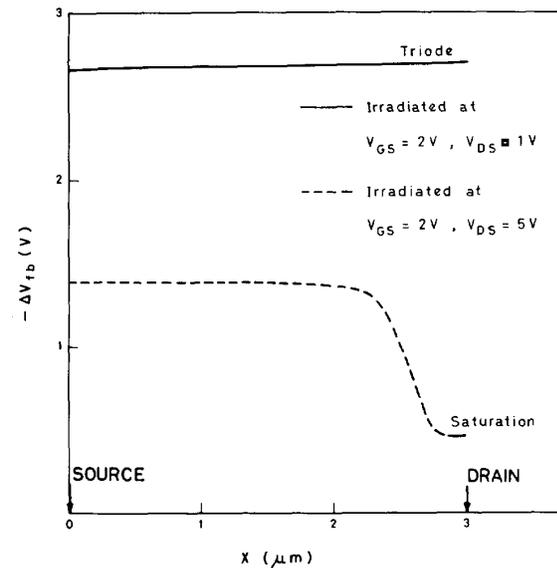


Fig. 6. The flatband voltage shift across the channel for an *n*MOS transistor biased in the triode region (Total dose of 1 M rad(Si)) and the saturation region (Total dose of 200 k rad(Si)) during irradiation. The effective channel length is 3 μm and the dose rate used was 100 rads (Si)/s. The oxide thickness is 500 Å. The peak trap density is  $5 \times 10^{18}/\text{cm}^3$ , the width of the gaussian distribution is 50 Å and the location of the centroid is at 100 Å. The values of the capture cross sections are mentioned in the text.

hence the drain current in the device. However, in this case the threshold voltage at the drain end is lower than at the source end and the drain region will therefore get inverted at a lower gate voltage. Therefore, by the time the source gets inverted, there is already a lot of inversion layer charge near the drain end, leading to currents that are larger than expected from the threshold voltage shift ( $\Delta V_T$ ). This can be seen more clearly from curves (a) of Fig. 7, which shows the inversion layer charge for two cases. The dashed line is the inversion charge for an MOS transistor that contains a laterally uniform fixed oxide charge that will give rise to a threshold voltage approximately equal to the threshold voltage at the source after irradiation. The solid line is the inversion charge obtained after irradiation in the triode region. Both the curves are obtained at  $V_{GS} = 0$  V and  $V_{DS} = 2$  V. It is clearly seen that the inversion charge at the drain end is increased due to lower thresholds at the drain, thus giving rise to higher currents. Fig. 8 shows the *I-V* characteristics of the device before and after irradiation, and it is seen that due to the nonuniformity in the lateral charge, the currents after irradiation are higher than expected from the threshold voltage shift. Since the difference in the threshold voltages at the two ends is not very large, the increase in current is not significant in the triode region, but is significant in the saturation region, when the inversion layer charge at the drain end is lower. As expected, the subthreshold characteristics show a parallel shift as seen in Fig. 9.

As seen in Fig. 6, *n*-MOS transistors irradiated in saturation show a much larger nonuniformity in the oxide charge across the channel. Since the oxide fields near the drain end, close to the drain depletion region is negative (the field lines point

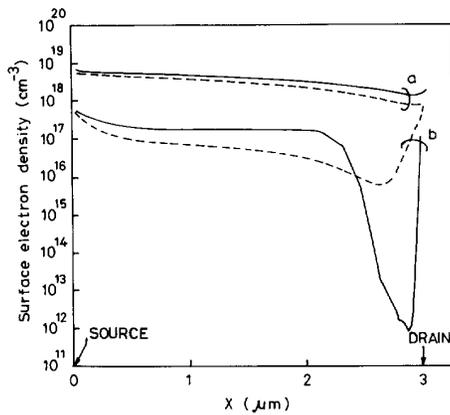


Fig. 7. The inversion charge along the interface for the transistors irradiated in the triode and saturation region. The dashed lines show the inversion charge in an MOS transistor that contains a laterally uniform fixed charge that results in a threshold voltage approximately equal to the threshold voltage at the source after irradiation. The solid line in (a) is the inversion charge obtained after irradiation in the triode region. Both the curves in (a) are obtained for  $V_{GS} = 0$  V and  $V_{DS} = 2$  V. The solid line in (b) is the charge obtained after irradiation in the saturation region. The two curves in (b) are obtained for  $V_{GS} = -0.7$  V,  $V_{DS} = 0.25$  V.

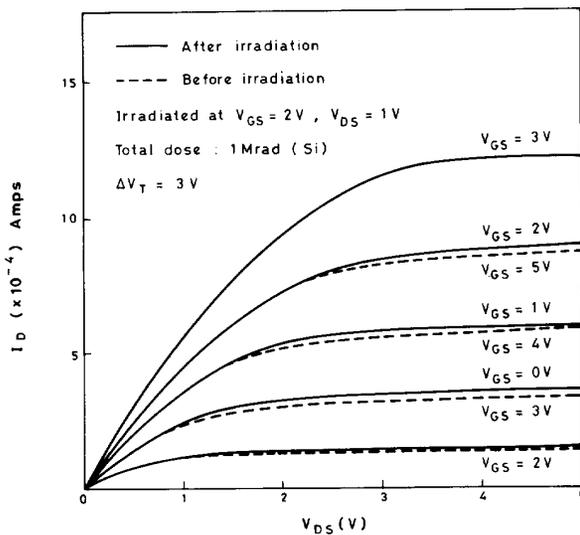


Fig. 8. The output characteristics of an  $n$ -channel transistor before and after irradiation. The transistor was biased in the triode region during irradiation. The total threshold voltage shift due to radiation is 3 V. The peak trap density is  $5 \times 10^{18}/\text{cm}^3$ , the width of the gaussian distribution is 50 Å and the location of the centroid is at 100 Å. The values of the capture cross sections are mentioned in the text.

towards the gate), the amount of trapped charge is much lower near the drain (since the generated holes drift towards the gate and the hole traps are located near the interface). This gives rise to a higher threshold voltage at the drain end and at the gate voltage corresponding to  $V_T$  at the source end, the drain does not get inverted at all, as seen in curves (b) of Fig. 7. Once again, the dashed line is the inversion charge in an MOS transistor that has laterally uniform oxide charge that gives rise to a threshold voltage that is equal to the threshold voltage at

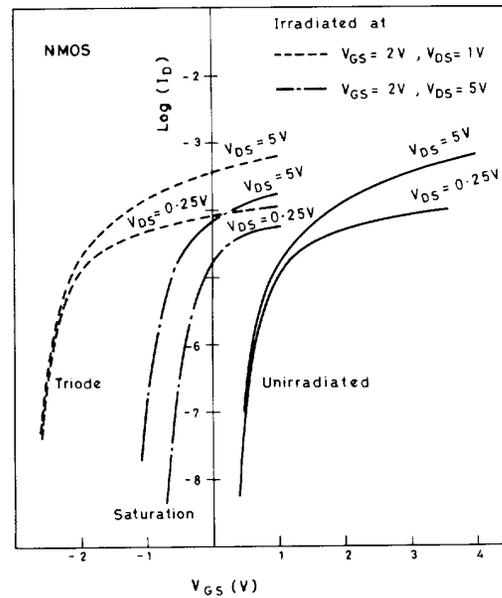


Fig. 9. The subthreshold characteristics before and after irradiation in the triode region ( $V_{GS} = 2$  V,  $V_{DS} = 1$  V, Total dose: 1 Mrad (Si)) and in the saturation region ( $V_{GS} = 2$  V,  $V_{DS} = 5$  V, Total dose: 200 k rad (Si)). The effective channel length is 3 μm. The peak trap density is  $5 \times 10^{18}/\text{cm}^3$ , the width of the gaussian distribution is 50 Å and the location of the centroid is at 100 Å. The values of the capture cross sections are mentioned in the text.

the source after irradiation. The solid line shows the inversion charge that is obtained after irradiation in the saturation region, and obviously the drain does not get inverted at all. A slightly larger gate voltage is needed to get significant current in the device. It can be seen from Fig. 9 that after irradiation, the subthreshold current increases significantly with the drain bias. This gives rise to a threshold voltage that depends on the drain bias during measurement as shown in Fig. 10. As seen from the figure, the threshold voltage decreases with an increasing drain bias and approaches the threshold voltage at the source end at larger drain voltages. This can be explained as follows. Over most of the channel, the oxide field is largely due to the gate voltage. Very near the drain junction however, the oxide field is determined both by the drain and the gate voltages. This gives rise to a more or less uniform buildup of charge over a large portion of the channel and a steep nonuniformity in the charge very near the drain junction, as seen in Fig. 6, which shows the resulting flatband shift. At large drain biases, this high-threshold region near the drain is completely covered by the drain depletion region and hence it does not affect the threshold voltage of the device, which is then determined by the source threshold. However, at low drain biases the drain depletion region does not cover the high-threshold region completely and consequently a portion of the channel does not get inverted at the gate voltage corresponding to the threshold at the source. This gives rise to a higher threshold voltage for the device if measured at low drain biases.

Since the extent of the high-threshold region near the drain depends on the drain depletion width during irradiation, it will

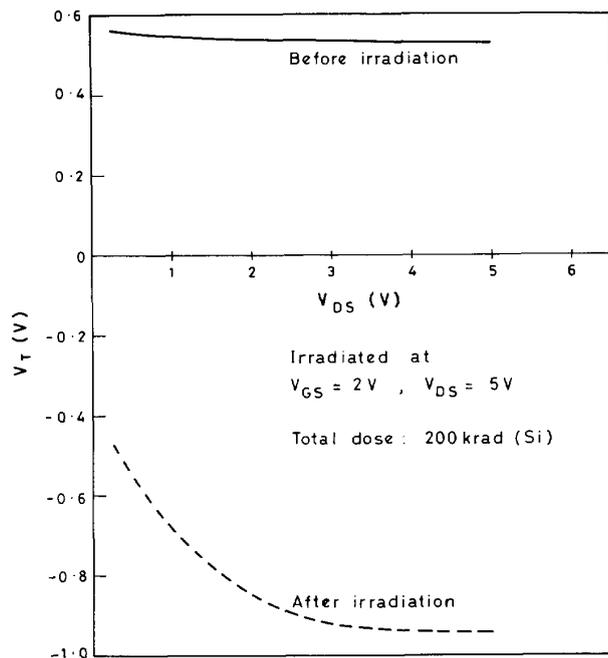


Fig. 10. The threshold voltage variation with the drain voltage during measurement for the  $3 \mu\text{m}$   $n$ -channel transistor irradiated in the saturation region. The peak trap density is  $5 \times 10^{18}/\text{cm}^3$ , the width of the gaussian distribution is  $50 \text{ \AA}$  and the location of the centroid is at  $100 \text{ \AA}$ . The values of the capture cross sections are mentioned in the text.

vary with the applied gate and drain voltage during irradiation. A higher gate voltage during irradiation will therefore result in a lower nonuniformity in the charge. This in turn would lead to a smaller variation in  $V_T$  with the drain bias during measurement as seen in Fig. 11. Also, with an increase in the total dose, the nonuniformity in the charge increases, resulting in a larger  $V_T$  variation with the drain bias during measurement as shown in Fig. 11.

Fig. 12 shows the output characteristics of the  $n$ -channel device before and after irradiation in the saturation region. From the figure, it can be seen that there is a significant difference in the currents before and after irradiation at the same  $V_{GS} - V_T$ . Also it becomes more difficult to drive the device into saturation after irradiation. This is because as the pinch-off region goes further into the channel, the edge of the channel sees an increasing gate voltage due to an increasing amount of positive charge in the oxide (as seen from Fig. 6), resulting in an increasing drain current. This is consistent with the fact that the threshold voltage decreases with the applied drain voltage during measurement.

$P$ -channel devices that are irradiated when biased in either the triode or saturation region, have a larger amount of positive charge near the drain end of the channel. This is because in a  $p$ -channel device, the oxide fields become more positive going towards the drain, irrespective of whether the transistor is biased in the triode or saturation region. Since the threshold voltage at the drain end is larger (i.e., more negative) than at the source end, the value of  $V_T$  decreases (i.e., becomes less

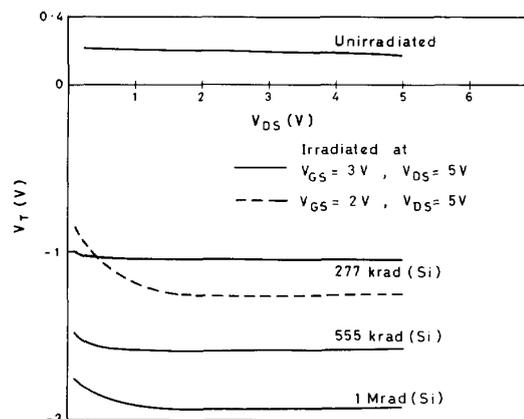


Fig. 11. The threshold voltage variation with the drain voltage during measurement for different values of the total dose. This is for an  $n$ MOS transistor irradiated in the saturation region ( $V_{GS} = 3 \text{ V}$ ,  $V_{DS} = 5 \text{ V}$ ). Also shown is the threshold variation for the transistor irradiated deeper in the saturation region ( $V_{GS} = 2 \text{ V}$ ,  $V_{DS} = 5 \text{ V}$ ), for a total dose of  $277 \text{ krad(Si)}$ . The effective channel length is  $1.5 \mu\text{m}$ . The peak trap density is  $5 \times 10^{18}/\text{cm}^3$ , the width of the gaussian distribution is  $50 \text{ \AA}$  and the location of the centroid is at  $100 \text{ \AA}$ . The values of the capture cross-sections are mentioned in the text.

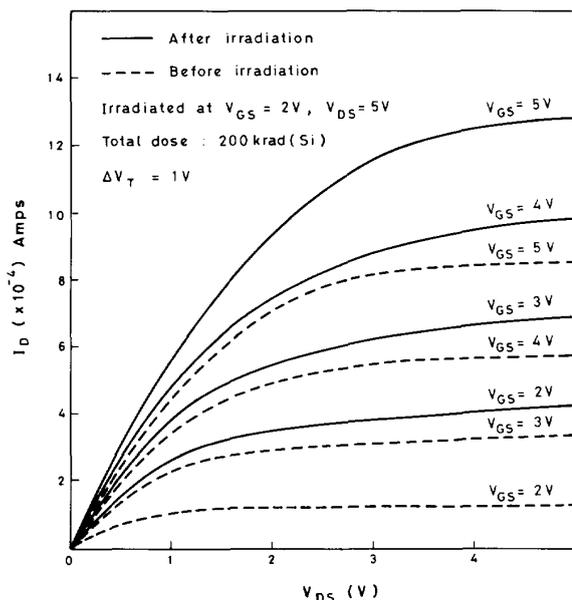


Fig. 12. The output characteristics of an  $n$ -channel transistor ( $L_{EFF} = 3 \mu\text{m}$ ), before and after irradiation. The transistor was biased in the saturation region during irradiation. The total threshold voltage shift due to radiation is  $1 \text{ V}$ . The peak trap density is  $5 \times 10^{18}/\text{cm}^3$ , the width of the gaussian distribution is  $50 \text{ \AA}$  and the location of the centroid is at  $100 \text{ \AA}$ . The values of the capture cross sections are mentioned in the text.

negative) with an increasing drain bias during measurement, the characteristics of this variation being similar to  $n$ -channel devices irradiated when biased in saturation.

Preliminary measurements on irradiated CD 4007  $p$ MOS transistors in our laboratory show that the threshold voltage after irradiation varies with the drain bias during measurement

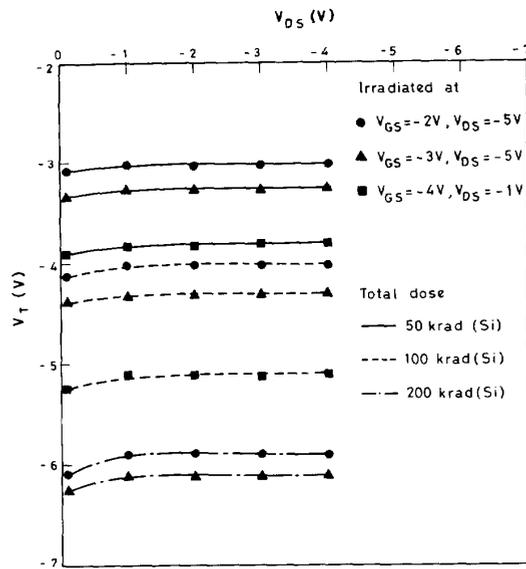


Fig. 13. The threshold voltage variation with the drain voltage during measurement for irradiated CD4007 *p*-MOS transistors in the saturation region ( $V_{GS} = -2$  V,  $V_{DS} = -5$  V and  $V_{GS} = -3$  V,  $V_{DS} = -5$  V) and triode region ( $V_{GS} = -4$  V,  $V_{DS} = -1$  V) at different values of the total dose.

[19]. This is shown in Fig. 13 for two transistors irradiated in the saturation region ( $V_{GS} = -2$  V and  $-3$  V,  $V_{DS} = -5$  V) and one in the triode region ( $V_{GS} = -4$  V,  $V_{DS} = -1$  V). It can be seen that the threshold voltage varies with the drain bias during measurement for transistors irradiated in the triode and saturation region, as expected. The amount of variation in the threshold voltage decreases with an increasing gate bias during irradiation in saturation region. It also increases with increasing dose, as expected from the simulations. However, the transistor irradiated in the triode region shows a variation in  $V_T$  that is larger than expected, which could be due to interface state generation. Exact comparisons are not possible as the doping profile, oxide thickness etc. are not known exactly and also because all of these transistors also showed some amount of interface state generation.

## V. CONCLUSION

We have, for the first time, developed a two-dimensional time-dependent simulator that solves all the equations in both the oxide and the semiconductor. Simulations were performed to obtain the oxide charge due to radiation under various bias conditions. When no drain bias is applied during irradiation, the results compare well with experiment. However a good correlation with flatband shifts in capacitors is obtained only for low total doses and large values of the applied gate bias during irradiation. A drain bias during irradiation results in a nonuniform charge buildup across the channel and this results in a threshold voltage after irradiation, that depends on the drain bias during measurement. This is also seen in transistors subject to hot carrier degradation [20]. Measurements of the oxide charge and interface states close to the source and drain depletion regions have been made in transistors

irradiated both with and without drain biases [21]–[22]. In both cases, a nonuniformity in the charge has been observed arising due to a varying electric field in this region. However exact comparisons would require reasonably accurate doping profiles near the source and drain junctions which are not available. Also, preliminary data on irradiated CD4007 PMOS transistors showed some of the trends predicted by the simulator.

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