A novel converter topology for TEM applications

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Abstract. Time-domain Electro Magnetic (TEM) systems, are used for remote sensing of conductive mineral deposits buried under the surface of the earth. A low frequency trapezoidal current excitation set-up in an exciter coil loop causes a flux that penetrates deep into the earth. When the excitation is cut off sharply, conductive deposits in the earth carrying flux react by causing eddy current flows within them. The flux produced by such eddy currents is picked up by a sensor coil. By comparing the emf induced in the sensor coil with *a priori* known emf patterns for mineral deposits, the presence of mineral deposits can be ascertained. The voltage, current and energy levels of the TEM system, require special type of excitation technique.

Power converters for such non-standard requirements are not reported in the literature, particularly for TEM applications. This paper introduces TEM systems to the reader and presents the requirements for excitation. A converter topology to meet the requirements, it's analysis, control and performance are presented. Among other alternatives that the authors have attempted, the topology presented features reduced number of passive elements, high voltage gain and low losses. These features enable the sensor head to be operated from the normal low level battery.

Keywords. TEM; transmitter; excitation; converter; topology.

1. Introduction

Electromagnetic methods (USACE 1995; Fountain 1998) are extensively used by Geophysicists in mineral exploration. The principle can be understood with reference to figure 1 which shows an arrangement of transmitter and receiver coils. The transmitter is excited with an electric current, setting up a flux (primary flux) that penetrates sufficiently deep below the earth's surface. A fraction of the primary flux links with the receiver coil. If the transmitter coil current is changed, the flux linking the coils changes, resulting in an emf being induced in the receiver coil. Let this emf be $e_P(t)$. Let there be a conductive material/body (conductivity of typically 100 times that of the surrounding media) in the path of the primary flux below the earth's surface as shown in figure 1. When the current in the transmitter coil changes, emf is also induced in the conductive body, establishing eddy currents, thus creating a secondary flux. A portion of the secondary flux links with the receiver coil. So the receiver coil sees a net flux due to both primary and secondary flux. Let the resulting emf in receiver coil

be $e_{PS}(t)$. A difference in these emfs $e_{PS}(t) - e_P(t)$ indicates the presence of a conductive body anomaly. An interpretation (Ravenhurst 2001) of such induced emfs is an established procedure, leading to the identification of the conductivity anomaly to be of a particular material, at a certain depth, dip and volume. Based on the nature of the excitation currents, such detection systems are classified as frequency domain (FEM) or time domain systems (TEM). Of them, TEM systems provide feasibility for greater exploration depths (Geotechairborne 2007a) and are either airborne (Fountain 1998), semi-airborne or ground based (Smith *et al* 2001). TEM systems flown by helicopters (HTEM) (Sattel 2006; Sorensen and Auker 2004) as in figure 1 are preferred. This paper is concerned with power electronics for excitation in HTEM systems.
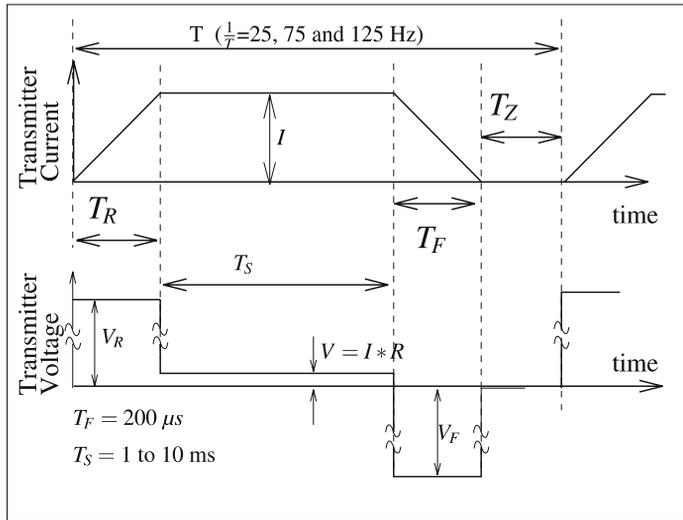
1.1 *HTEM System requirements*

The transmitter coil of a HTEM system consists of few turns, typically circular in shape with diameters up to 25 m. The receiver is a coplanar, concentric coil with much less diameter and having several turns. TEM systems typically use half-sine, triangular, square or trapezoidal current waveforms. Trapezoidal current (Geotechairborne 2007b) excitation is preferred, whose waveform is shown in figure 2. The excitation requirements are as follows;

- establish a steady current in the transmitter
- abruptly reduce this current to zero and
- record the receiver coil voltage (after the transmitter transmitter current falls to zero, for a duration of 1 ms to 10 ms) for off-line signature analysis and mineral detection at that location.

The current pulse through the coil has a short rise time (T_R) of about 200 μs. Constant current is maintained in the coil for a certain duration ($T_S = 1$ ms to 10 ms). The current
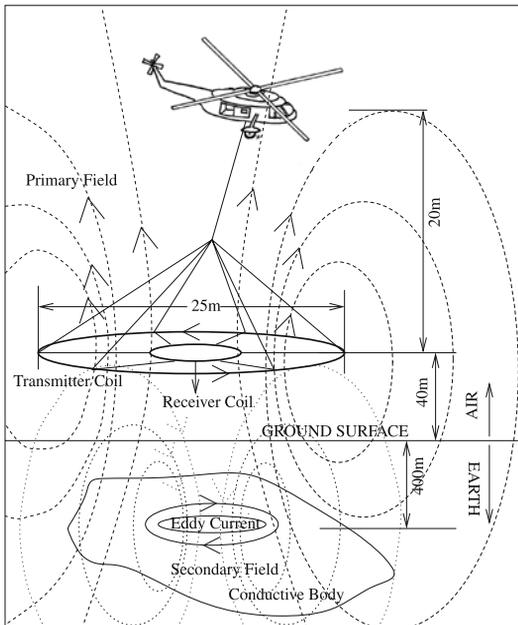
Figure 1. The helicopter TEM (HTEM) system.

Figure 2. Voltage requirement of the transmitter coil of TEM system.

through the coil is then switched OFF and the fall time (T_F) is regulated to 200 μs. Larger exploration depths require that the excitation current have larger amplitude and smaller fall time. After a zero current interval (T_Z), the cycle repeats at 25/75/125 Hz rate. In the laboratory scale implementation presented in this paper, the transmitter coil inductance 'L' is 940 μH, current amplitude (I) is taken to be 30 A, and the source voltage 12 V. In an actual full scale implementation, $L = 3$ mH, $I = 300$ A, requiring $V_R = V_F = 4500$ V (these being the voltage across the transmitter coil during current rise and fall times respectively; see figure 2, while the typical supply voltage may be about 100 V.

This paper proposes a novel converter topology to meet these excitation current requirements. A novel control method 'leading edge modulation' is proposed to stabilize the dc bus voltage. The topology permits the operation of TEM systems requiring several kilo volt excitation directly from a low voltage battery. Section 2 describes the proposed topology, the operating modes, current control and voltage control. The capacitor voltage dynamics' modelling, and the overall control scheme are discussed in § 3. The experimental results from the laboratory prototype are presented in § 4. Finally, the conclusions drawn are presented in § 5.

2. Proposed topology and modes of operation

The proposed converter topology is shown in figure 3a. The R-L load represents the transmitter coil. The operation of the circuit can be divided into 4 modes (shown in figure 3) as follows.

2.1 *Modes of operation*

2.1a *Mode-1:* This, first operating mode in a cycle, starts with the required voltage across the capacitor. Switches S_A and S_{AB} are turned ON and the load current increases from zero to I in time T_R.
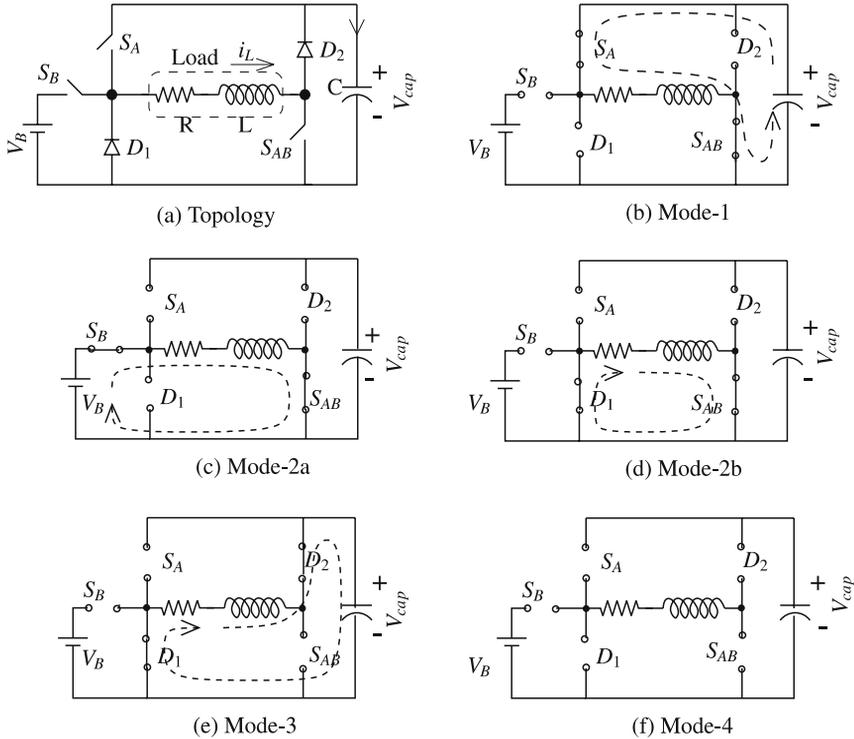
Figure 3. Proposed topology.

2.1b *Mode-2:* Switching OFF of S_A initiates this mode. S_B, D_1 are operated cyclically resulting two sub-modes; Mode-2a and Mode-2b, correspondingly when each of them is ON and the other is OFF. During this interval the load current is maintained at an average value I.

2.1c *Mode-3:* At the end of second interval, all controlled switches are turned OFF. Due to the inductive nature of the load, the diodes D_1 and D_2 are forced into conduction mode, and the converter enters the Mode-3 of circuit operation. The capacitor voltage forces the load current to fall and reverse its direction. Since the diodes cannot conduct the reverse current, they are commutated to OFF state and circuit enters Mode-4.

2.1d *Mode-4:* All switches and diodes are in OFF state and load current is zero for the entire interval. Then this cycle repeats.

2.2 *Converter current control*

The converter control system is given a square wave current reference of required amplitude, ON duration T_S and frequency. The cycle starts with the current reference going high and the circuit enters Mode-1. S_A and S_{AB} are switched ON. The capacitor voltage appears across the load and current increases linearly. When the load current reaches I, Mode-1 ends and Mode-2 begins. During Mode-2, S_{AB} is ON for the entire interval. Switch S_B and diode D_1 are used to regulate the load current. In this implementation, simple hysteresis control is used for this purpose. When the current reference goes zero, the circuit enters Mode-3. There is a
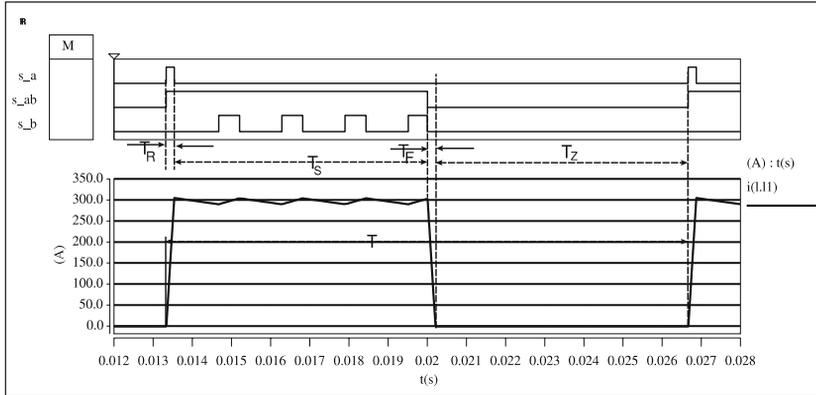
Figure 4. Load current: Simulated result from SABER.

finite time taken by the load current to fall to zero in this mode. A typical waveform is shown in figure 4.

2.3 *Capacitor voltage control*

During Mode-1, the capacitor (with an initial voltage of V_{TRF}) is connected across the load, until the load current increases to I. The energy E_{loadTR} transferred to L is $0 \cdot 5LI^2$. During this process, some finite energy is collectively lost in R (the equivalent load resistance), and in the drops across S_A and S_{AB}. So the capacitor effectively loses an energy E_{TR} during Mode-1. Similarly during Mode-3, the load energy is transferred to the capacitor. But some energy is lost in the process in R, the load resistance and in diodes D_1 and D_2. Thus effectively E_{TF} is gained by the capacitor. If $E_{TR} > E_{TF}$, the capacitor effectively loses energy and the voltage falls to reflect this loss. Similarly if $E_{TR} < E_{TF}$, the capacitor gains energy over the cycle and accordingly the voltage goes up. During steady state one has to ensure that $E_{TR} = E_{TF}$ for steady capacitor voltage and hence there is a need for regulating the capacitor voltage.

Further, The current fall time T_F is a critical requirement. Since the capacitor voltage dictates the fall time, it is to be well regulated. When the current amplitude changes, the capacitor voltage also needs to be set to a appropriate value. Control of capacitor voltage required on account of this requirement also. The capacitor voltage can be controlled by controlling E_{TR} and E_{TF}. E_{TR} can be controlled by controlling the duration of T_R. By reducing T_R, we can reduce E_{TR} and vice versa. Similarly E_{TF} can be controlled by controlling the duration of T_F. In the present application, the requirements during T_F are critical. So T_F is not modified. Only T_R is changed by an acceptable amount. This technique is termed as *Leading Edge Modulation*, as shown in figure 5. In the figure, the single shaded regions correspond to the intervals when the capacitor discharges into the load. When the capacitor voltage is desired to be increased, this interval is lesser than ideal, while it is higher if we would like to reduce the voltage. Though this would mean that the load current is not the steady value of I at the end of mode-1, the surplus/deficit is removed by the subsequent hysteresis operation of mode-2. This is shown by the cross hatched regions in figure 5. Since the current fall interval is the same, the capacitor charging time is not affected. Thus while E_{TF} is not changed, E_{TR} is controlled to affect the net energy lost/gained by the capacitor. In this manner, by controlling the leading edge of the load current pulse, the capacitor voltage control is attempted in this work. The capacitor voltage dynamics need to be modelled so as to regulate/track the changes
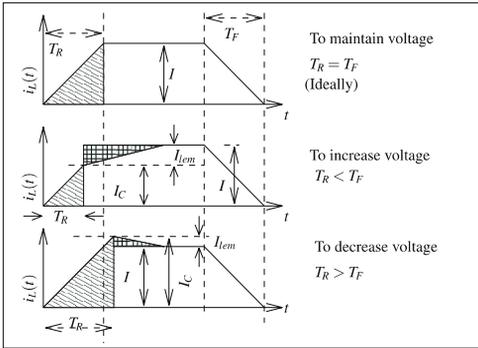
Figure 5. Leading edge modulation.

in current. The modelling of the system dynamics when using leading edge modulation is presented in the next section.

3. Modelling the capacitor voltage dynamics

The typical load current and capacitor current are shown in figure 6. The capacitor current as shown is discontinuous. Principles of converter analysis are presented in Mohan *et al* (2003). Erickson & Maksimovic (2005) discusses modelling conventional converters, Jian *et al* (2001) discusses modelling of converters in discontinuous conduction mode. For the current hysteresis controller, the current reference during Mode-2 is I, while for intervals T_F and T_R the current reference is zero. With Leading Edge Modulation, the capacitor voltage is to be controlled by varying T_R interval. An easy way to adjust T_R (with same hysteresis controller used in the other modes) to vary the level of the reference current during Mode-1. Let the current for the hysteresis controller during Mode-1 be I_C. To effect an increase in the capacitor voltage, I_C is decreased and vice-versa. Mode-1 ends when load current reaches I_C (instead of I). In Mode-2, the hysteresis controller acts to bring the load current to I and so the load current at the beginning of Mode-3 is I. The Hysteresis current controller thus acts in a way to remove the effects of the load inductance on the dynamics of the capacitor voltage. If $\langle i_{cap}(t)\rangle_T$ is the average capacitor current and $\langle v(t)\rangle_T$ is the average capacitor voltage over the interval T, then the dynamics of the capacitor voltage (neglecting resistance and other
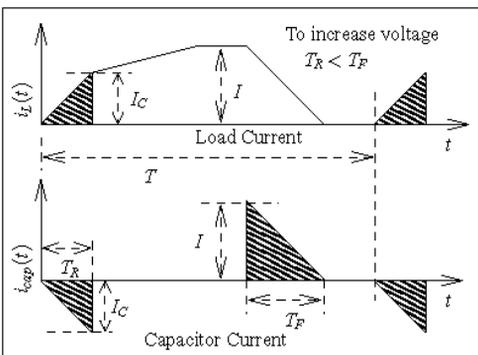

Figure 6. Capacitor voltage dynamics.

losses in the circuit) is given as follows.

$$\langle i_{cap}(t)\rangle_T = C\frac{d}{dt}[\langle v(t)\rangle_T]. \tag{1}$$

The average capacitor current can then be computed from the net area under the triangles during one cycle in figure 6 as

$$\langle i_{cap}(t)\rangle_T = \frac{1}{T}\left[-\int_0^{T_R}\frac{V_{TRF}}{L}\tau d\tau + \int_0^{T_F}\left(I - \frac{V_{TRF}}{L}\tau\right)d\tau\right]. \tag{2}$$

After evaluating the integral (capacitor current rises and falls linearly with time),

$$\langle i_{cap}(t)\rangle_T = \frac{1}{T}\left[-\frac{V_{TRF}}{2L}T_R{}^2 + IT_F - \frac{V_{TRF}}{2L}T_F{}^2\right], \tag{3}$$

where $V_{TRF} = \langle v(t)\rangle_T$, the average capacitor voltage, $T_R = (LI_C/V_{TRF})$ and $T_F = (LI/V_{TRF})$. Simplifying (3),

$$\langle i_{cap}(t)\rangle_T = \frac{L}{2T\langle v\rangle_T}[I^2 - I_C{}^2]. \tag{4}$$

From (3) and (4), we get

$$C\frac{d}{dt}[\langle v\rangle_T] = \frac{L}{2T\langle v\rangle_T}[I^2 - I_C{}^2]. \tag{5}$$

Rearranging the above equation, we get (6), the model for the capacitor voltage dynamics.

$$\frac{2TC}{L}\langle v\rangle_T\frac{d}{dt}[\langle v\rangle_T] = [I^2 - I_C{}^2]. \tag{6}$$

This is an averaged large signal model which is nonlinear and has to be linearized about an operating point to get a small signal model for the purpose of control. This is done by applying small signal perturbations.

Under steady state conditions, the average capacitor voltage does not change, and $I = I_C$. Now let the system be perturbed so that,

$$\langle v\rangle_T = V + \hat{v} \tag{7}$$

$$\langle I\rangle_T = I + \hat{i} \tag{8}$$

$$\langle I_C\rangle_T = I_C + \hat{i_C}, \tag{9}$$

where $\hat{v}, \hat{i}$ and $\hat{i_C}$ are the small signal perturbations. Then (6) is evaluated as follows.

$$\frac{2TC}{L}(V + \hat{v})\frac{d}{dt}[(V + \hat{v})] = [(I + \hat{i})^2 - (I_C + \hat{i_C})^2] \tag{10}$$

$$\Rightarrow \frac{2TC}{L}(V)\frac{d}{dt}\hat{v} + \frac{2TC}{L}(\hat{v})\frac{d}{dt}\hat{v} = 2I(\hat{i} - \hat{i_C}) + [(\hat{i})^2 - (\hat{i_C})^2]. \tag{11}$$

Neglecting the higher order terms, we get

$$\frac{2TCV}{L}\frac{d}{dt}\hat{v} = 2I(\hat{i} - \hat{i}_C). \tag{12}$$

Taking the Laplace transform,

$$\frac{TCV}{L}s\hat{V}(s) = I[\hat{I}(s) - \hat{I}_C(s)] \tag{13}$$

$$\hat{V}(s) = \frac{T_F}{TCs}[-\hat{I}_C(s) + \hat{I}(s)], \tag{14}$$

which is the small signal ac model of the system. We can see that the representation is that of an integrator. $\hat{I}_C(s)$ is the control input since it directly determines T_R. $\hat{I}(s)$ is considered as a disturbance input as far as this control loop is concerned.

3.1 *Control structure*

A simple feedback controller for the capacitor voltage control is shown in figure 7. The variables with a '*' superscript indicate reference quantities. The plant model equations are included in a block diagrammatic format in this figure, showing $\hat{I}_C(s)$ as the control input and $\hat{I}(s)$ as a disturbance. The voltage controller generates the current reference I_C^*, used by the controller during Mode-1. In the actual system, the current reference I^* is set by the user depending on the depth of exploration. The capacitor voltage has to adjust to fulfil the fall time requirement. Hence the voltage reference is obtained from the current reference I^*. As $\hat{I}(s)$ acts as a disturbance to the voltage control loop, but since a measure of it is available, a modified, feed forward controller as in figure 8 can be used to improve the dynamics of the system. This structure aims to cancel the effects of $\hat{I}(s)$ on the plant. The controllers designed are simple proportional controllers, since the plant is already of integrating type. Figure 9 compares the response obtained from the small signal equations and actual circuit simulation, both in closed loop for a full scale model. The experiment corresponds to a step change in current reference I^*. The figure shows the current through the exciter coil from actual circuit simulation (bottom trace), and compares the voltages across the capacitor from circuit simulation and small signal model. The first step at t=0 is a large signal disturbance. It can be seen that while the nature of response of the capacitor voltage is similar, the rise
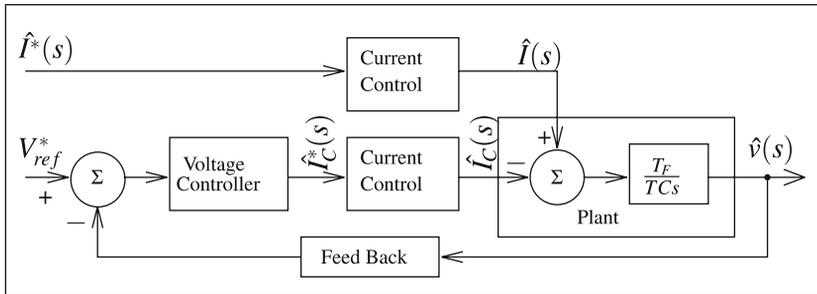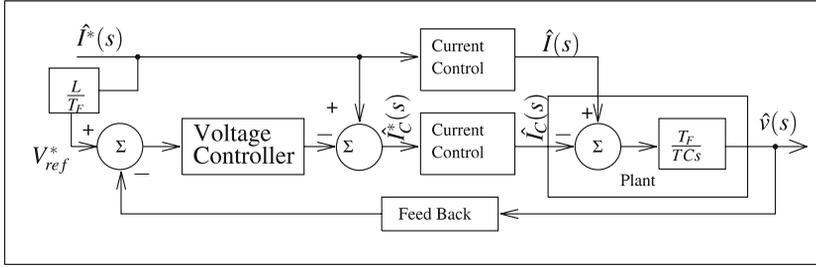

Figure 7.   Voltage controller.

Figure 8. Feed forward controller.

times are different. The model is clearly not able to predict large signal effects. The second transient shown is a small current step at $t = 0.5$ s. In this case it can be seen that the small signal model is able to accurately predict the circuit simulated voltage in dynamics and steady state. This validates the modelling effort and the control performance.

4. Experimental results

A laboratory scale prototype of the transmitter (2·5 m diameter, 3 turns) and the power converter ($I = 30$ A) were fabricated to validate the proposed topology and control structure. For these parameters, the prototype design values and components are as follows;

$C = 2200\,\mu$F, $L = 940\,\mu$H, $R = 0.13\,\Omega$

$S_{A,B,AB} = $ MOSFET, 200 V, 60 A, $D_x = $ ULTRA FAST diodes, 200 V, 60 A

$k_p = 4$, $f = 25, 75, 125$ Hz, selectable, $T_F = 200\,\mu$s, $T_{Smin} = 1$ ms

$I = $ up to 30 A, $V_B = 12$ V, $T_{Smax} = 10$ ms @25 Hz, 80% duty cycle @75, 125 Hz.
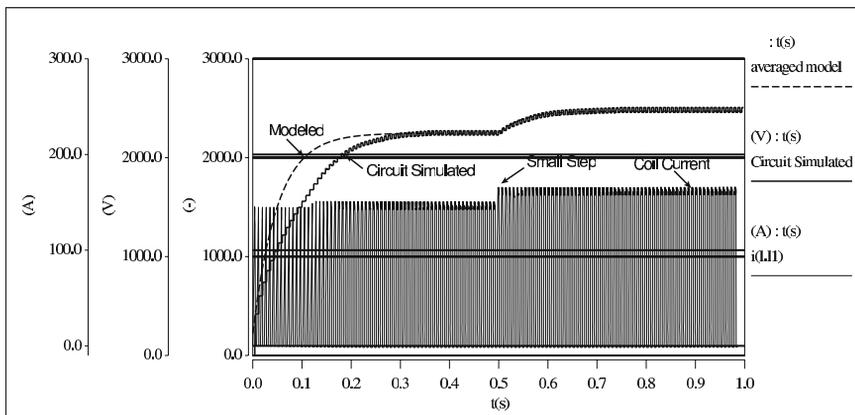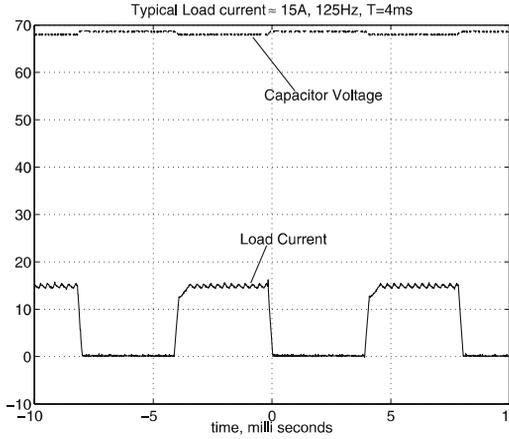

Figure 9. Model, controller validation, closed loop.

Figure 10. Typical load current.

4.1 *Typical load current*

The load current and the corresponding capacitor voltage ($\approx$ 15 A, 125 Hz, $T_S = 4$ ms) is shown in figure 10. The fast rise/fall in load currents during T_S and T_F can be seen. The ripple seen on the load current waveform is due to the action of hysteresis control. It can be seen that the capacitor voltage drops at the beginning of the ON time due to energy outflow and regains voltage during turn OFF. It may be noted that even under steady state conditions, due to the losses in the converter, $I_C \neq I$. The two distinct slopes during the current rise, therefore, are a result of the leading edge modulation.

4.2 *Fall time*

The fall intervals for several different load current amplitudes are shown in figure 11. It can be seen that the fall durations are practically independent of the level of load current as desired at $200\,\mu$s. The corresponding modelled and experimental capacitor voltage variation with respect to load current is shown in figure 12. In all these experiments the battery voltage is maintained constant at 12 V. It can be seen that the capacitor voltage estimated, and measured

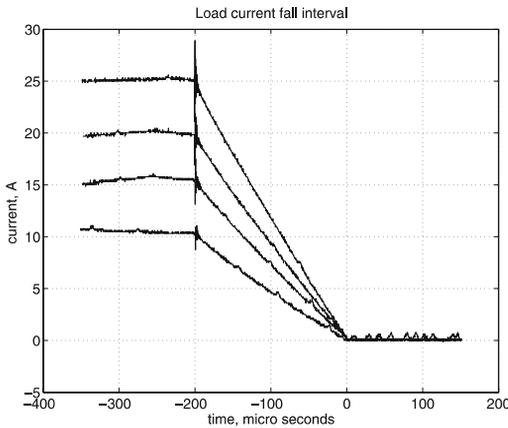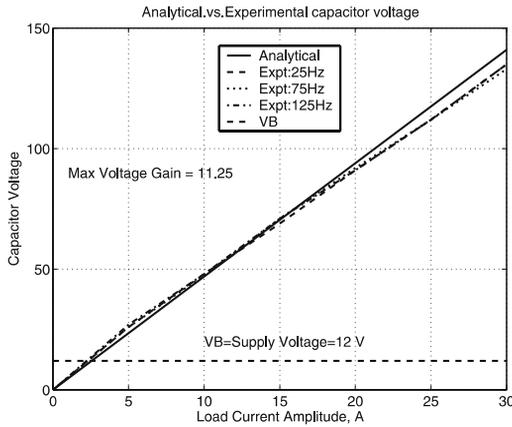**Figure 11.** Load current fall time.

Figure 12. Capacitor voltage.

match closely and increase with the current requirement linearly. Their independence on the frequency of operation is also clearly brought out in both model and experiment. The close match between the modelled and actual values of capacitor voltage and the constant fall times for varying load currents clearly validate the theory. The maximum voltage gain achieved is 11·25, which is high compared to the conventional boost converters.

4.3 *Power calculations*

In this topology, the low voltage dc source is used to supply the losses in steady state only, while the coil energy is recycled. In order to estimate the power requirements of this source, the estimated values are compared with experimental values in figure 13. In these computations, the estimated value is arrived at by taking into consideration device losses and coil resistance losses. The reasonably good match between the estimated and measured power requirements can form the basis of proper source selection in actual full scale implementations. In the other topologies that the authors explored or experimented with, the coil energy was dissipated in a resistor, while in the topology presented here, the coil energy is recycled leading to much lower power requirements.
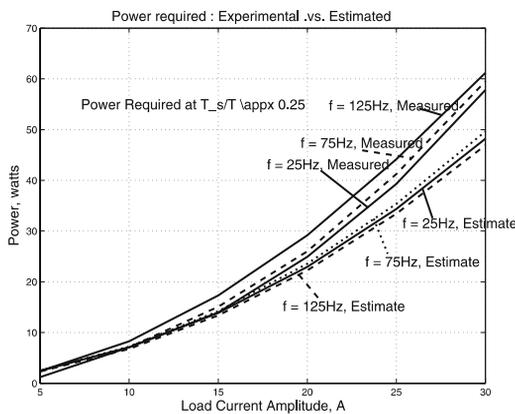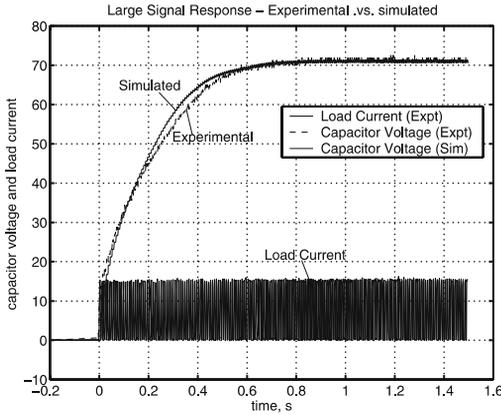

Figure 13. Power required.

Figure 14. Large signal response comparison.

4.4 *Transient response*

The simulated and experimental plots for a typical large signal change, a 50% load step from zero to 15 A, at $t = 0$ for $f = 125$ Hz, $T_S = 4$ ms, are shown in figure 14. The current is 125 Hz, 50% trapezoidal waveform (as in figure 10). But the time axis is large, the current appears as dark area in the figure. The circuit simulated and the experimental capacitor voltage can be clearly seen. This shows the close relation between the simulated and real world results. The simulated and experimental plots for a typical small signal change (current step from 15·5 A to 17·8 A, at $f = 125$ Hz, $T_S = 4$ ms s) are shown in figure 15. As in the large signal response, here again the current appears as dark area due its high frequency. The dynamic and steady state values from the circuit simulation and experimental are very close. This close match in capacitor voltages from simulation and experiment validate the converter modelling and control.

5. Conclusion

A new power converter topology, for TEM applications, was proposed. A new control technique *Leading Edge Modulation* was implemented. The converter was modelled and a simple
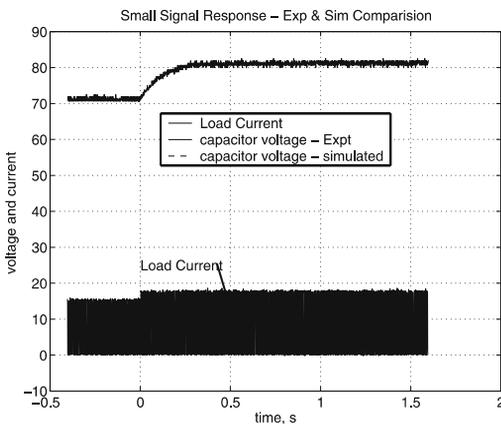

Figure 15. Small signal response comparison.

proportional control was proposed. For hardware implementation, a scaled down version was attempted. The performance of the topology was evaluated through simulation and experiments. The close match between the simulation and experimental results, validates the model and control technique developed. The low-loss nature of the circuit enables scalability for the full scale application also.

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