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A fully automated temperature-dependent resistance measurement setup using van der Pauw method

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The van der Pauw (VDP) method is widely used to identify the resistance of planar homogeneous samples with four contacts placed on its periphery. We have developed a fully automated thin film resistance measurement setup using the VDP method with the capability of precisely measuring a wide range of thin film resistances from few mΩ up to 10 GΩ under controlled temperatures from room-temperature up to 600 °C. The setup utilizes a robust, custom-designed switching network board (SNB) for measuring current-voltage characteristics automatically at four different source-measure configurations based on the VDP method. Moreover, SNB is connected with low noise shielded coaxial cables that reduce the effect of leakage current as well as the capacitance in the circuit thereby enhancing the accuracy of measurement. In order to enable precise and accurate resistance measurement of the sample, wide range of sourcing currents/voltages are pre-determined with the capability of auto-tuning for ∼12 orders of variation in the resistances. Furthermore, the setup has been calibrated with standard samples and also employed to investigate temperature dependent resistance (few Ω–10 GΩ) measurements for various chalcogenide based phase change thin films ($Ge_2Sb_2Te_5$, $Ag_5In_5Sb_{60}Te_{30}$, and In_3SbTe_2). This setup would be highly helpful for measurement of temperature-dependent resistance of wide range of materials, i.e., metals, semiconductors, and insulators illuminating information about structural change upon temperature as reflected by change in resistances, which are useful for numerous applications. *Published by AIP Publishing.* https://doi.org/10.1063/1.4998340

I. INTRODUCTION

Resistance measurement with the variation of temperature has received significant interest to the systematic characterization of the electronic transport properties of several materials including metals and semiconductors.[1,2] This type of measurement fulfills the demand of the standard procedure for technological development in semiconductor industry and electromechanical system engineering as well.[3] Moreover, this is a traditional way to classify the type of solids which is well matched with modern band theory.[4]

The van der Pauw (VDP) method is the popular way to identify the resistance of a sample with four contacts placed arbitrarily at the circumference.[5] This method excludes the contribution of parasitic contact resistance which provides the precise measurement of resistance.[6] Another important aspect of this method is that it is independent of the sample's shape. There are four important conditions that need to be fulfilled during the measurement using the VDP method: (a) the contacts are located at the circumference of the sample, (b) the area of contacts is small relative to the surface area of the sample, (c) the sample is homogenous in thickness, and (d) the sample does not contain isolated holes. However, condition (a) has some limitations to be achieved practically.[7] Initially, the errors related to the location of contacts from edge were discussed by van der Pauw.[8] Further, measurement accuracy is improved by selecting special sample shapes and contact placements.[9] The effect of finite contact size, contact placement, sample homogeneity with specific sample geometries including square, circle, and cloverleaf has already been systematically discussed in the literature.[10–12] Additionally, an analysis for contact size based on condition (b) has also been reported.[3] Recently, an interesting concept based on gated VDP is also discussed for electrical characteristics of thin semiconducting films.[13]

High temperature resistance measurement setups with the VDP method are also reported in the literature.[1,2,14,15] An *in situ* vacuum electrical resistivity measurement upon temperature is discussed to control efficient sputtering-oxidation coupling process for the fabrication of oxide compounds.[16] Another setup has also been used to understand thermal stability of thermoelectric materials via *in situ* resistivity measurement.[17] It is important to mention here that heat should be properly confined around the sample for temperature sensitive samples. For such a kind of application, a tubular furnace is the best as the heating zone is confined to a particular area with uniform distribution as well. Therefore, the efforts are needed for special designing of the sample holder, which can sustain high temperatures and would be worthwhile for resistance measurement with a tubular furnace. Moreover, detailed investigations on related electronics including switching network and automation for the VDP method have become a critical issue and need to be investigated properly.

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In this paper, we have developed a resistance measurement setup based on the VDP method that could be deployed inside a tubular furnace for high temperature application. We have designed a quartz based sample holder, which can be properly placed inside the tubular furnace. For multiple measurements across the sample after changing the source and sense terminals, a custom-built switching network board (SNB) is designed with minimum possible leakage current in the circuit. Moreover, sourcing the current/voltage is primarily decided by the instrument by means of predicting approximate range of resistance values using test signals; however, provisions have also been included such that the user could make a choice of source and measure values. The setup uses LabVIEW program to control all the sub-components of instrument and perform a real time temperature dependent thin film resistance measurement. The custom-designed setup provides numerous advantages compared to other systems reported in the literature.[1,15] This includes more accurate resistance measurement by means of employing all four configurations of van der Pauw geometry, simple design with provisions to pre-test the contact pads, user-friendly options for source/measure values, and a low cost solution of temperature-dependent resistance measurement based on the van der Pauw algorithm with high precision electronics including an indigenously built SNB. Furthermore, the developed setup has been used to investigate the resistance measurement upon temperature of $Ge_2Sb_2Te_5$ (GST), $Ag_5In_5Sb_{60}Te_{30}$ (AIST), and In_3SbTe_2 (IST) phase change materials.

II. SETUP DESCRIPTION

Figure 1 represents the block diagram of the temperature dependent resistance measurement setup. The setup mainly includes a sample holder, heating arrangement, and custom-built switching network with necessary electronic accessories.

A. Sample holder and heating arrangement

Tubular furnace with proportional integral differential (PID) temperature control which can heat the sample up to a maximum temperature of 600 °C with varying heating rate from 1 °C/min to 10 °C/min has been used. In order to avoid oxidation due to high temperature measurements and to load sample holder properly, quartz tube 1 is installed into the tubular furnace as shown in Fig. 1. One end of quartz tube 1 has a fixed inert gas inlet while the other end is open to load and unload the sample holder. The sample holder consists of a quartz plate of 40 mm × 40 mm connected with quartz tube 2. A quartz plate with four contacts using spring loading mechanism is used to enable the conducting path with contact-pads of samples. Quartz tube 2 encloses a cover along with provision for an inert gas (Ar) outlet so that it can be easily fixed inside quartz tube 1. One K-type thermocouple (*NI USB-TC01*) is clamped very close to the sample to obtain temperature of sample precisely. Moreover, four metal wires (W) have been taken out from the sample holder for resistance measurement as per the VDP method. These connections are drawn to *Keithley 2612B* source measure unit (SMU) via custom-built switching network.

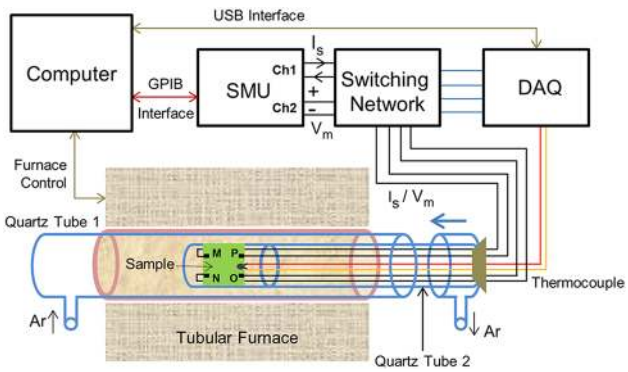

FIG. 1. Schematic of temperature dependent VDP resistance measurement setup. Tubular furnace is used to heat the sample, and a quartz based sample holder is designed for loading the sample at high temperature. Setup is fully automated and each instrument is controlled through LabVIEW.

B. Switching network board (SNB)

For the VDP method, interchanging the current and voltage terminal is the fundamental necessity. Moreover, the leakage current of the circuit and system time constant is also affected during measurement of highly resistive samples.[18] Therefore, a custom-built SNB has been designed to measure the resistance precisely as per the VDP geometry. A circuit schematic of the SNB is shown in Fig. 2. The SNB is designed by four silver contacts based SPDT relays, which are driven by transistor switches (SL100). Furthermore, source (Ch1) and measure (Ch2) terminals from SMU are fed into *A*, *B*, *C*, *D* ports of the board with a low noise shielded coaxial cable. To reduce the effect of leakage current and capacitance, proper guarding has been done using the inner shield of a coaxial cable with enabled guard port in *Keithley 2612B* SMU, which provide the buffered voltage that is at the same level as the input/output high voltage. Therefore, leakage current will not exist due to the absence of the differential voltage between two conductors in the cable and SMU will source and measure from device under test (DUT) only. Ports *A*, *B*, *C*, *D* are directly connected to relays, and different combinations of output are obtained at ports *M*, *N*, *O*, *P*. Digital outputs as control signals from *NI DAQ 6009* are given to the board at terminals *E*, *F*, *G*, *H* to operate the transistor. The operating voltage of the relay is 5 V, and when the low digital voltage control signal has been given, the transistor acts as an open circuit and the relays remain in *off* state. On the other hand, high digital voltage control signals activate the transistors and relays switch their position. In order to prevent the transistor from the reverse current of the relay coil, a freewheeling diode (1N4007) is connected parallel to the relay.

This setup is fully automated through LabVIEW where *Keithley 2612B* SMU and *NI DAQ 6009* are simultaneously controlled with a computer using a general purpose interface bus (GPIB) and universal serial bus (USB), respectively. Complete measurement has been performed in a controlled inert gas environment.

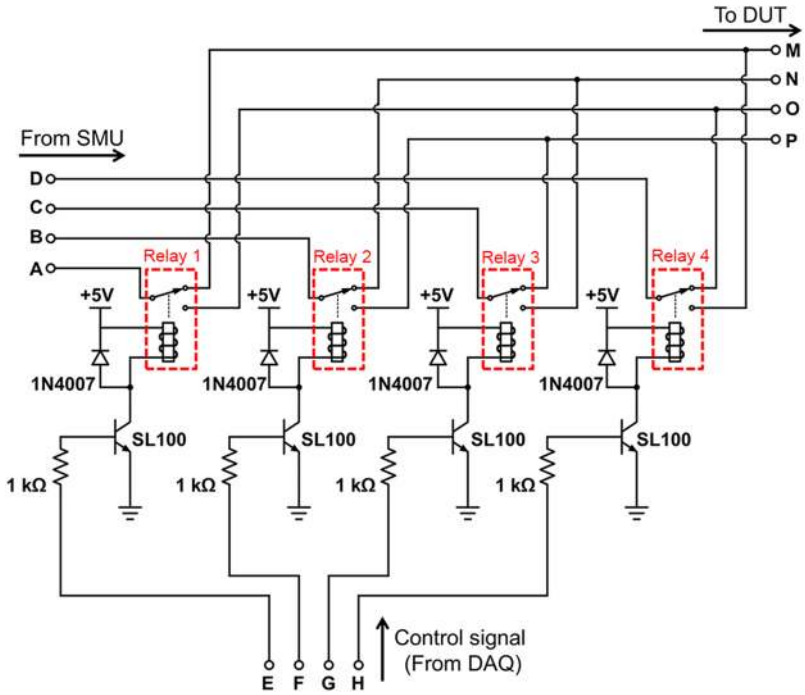

FIG. 2. Circuit diagram of the custom-built switching network board.

III. MEASUREMENT PROCEDURE

The sample connections of the traditional VDP method with four contacts, namely, *M*, *N*, *O*, *P* placed on the circumference of the DUT have been shown in Fig. 3. In general, for the source current I_{ij} between two adjacent contacts *i* and *j*, while measuring the voltage V_{kl} between two other contacts *k* and *l*, the resistance is given by $R_{ij,kl} = V_{kl}/I_{ij}$. Total four resistance values, namely, $R_{MN,PO}$, $R_{ON,PM}$, $R_{OP,NM}$, and $R_{MP,NO}$ are calculated as per the connections, which are presented in Fig. 3. Resistances $R_{MN,PO}$ and $R_{OP,NM}$ have the same value due to symmetry. However, measuring both resistance values and taking the average, R_A reduces the effect of imperfect contacts. Similarly, R_B is the average of other two resistance values $R_{ON,PM}$ and $R_{MP,NO}$. Furthermore, two resistances R_A and R_B fulfill the criteria of the VDP[5] mathematical formula

$$\exp\left(-\pi\frac{R_A}{R}\right)+\exp\left(-\pi\frac{R_B}{R}\right)=1. \quad (1)$$

Here R is the resistance of the DUT, which can be obtained after solving Eq. (1). Generally, R_A is different from R_B, due to which Eq. (1) cannot be solved analytically. Therefore, binary search or the Newton-Raphson-like standard numerical method is used to calculate the *R*.[1]

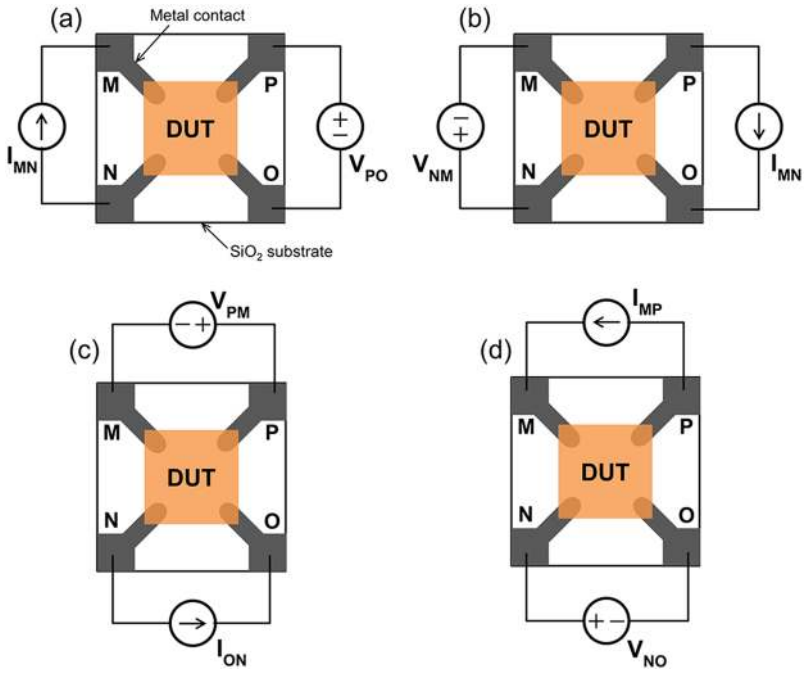

FIG. 3. Sample connections to identify the resistance according to the VDP method. Four connections from (a) to (d) with source and sense terminals have been mentioned to identify multiple resistance values.

TABLE I. Relay state as per connections required for van der Pauw geometry.

Connections	Relay state				Output
	Relay 1	Relay 2	Relay 3	Relay 4	
(a)	*off*	*off*	*off*	*off*	$R_{MN,PO}$
(b)	*on*	*off*	*off*	*on*	$R_{ON,PM}$
(c)	*on*	*on*	*on*	*on*	$R_{OP,NM}$
(d)	*off*	*on*	*on*	*off*	$R_{MP,NO}$

In order to obtain these four resistance values accurately, the SNB is configured as per the required connections. Table I contains the relay state according to the connections that have been shown in Fig. 3 and the corresponding resistance values as an output. For connection (a), all relays are in *off* state and then current I_{MN} is applied between contacts M and N, whereas voltage V_{PO} is measured at the contacts P and O. Resistance $R_{MN,PO}$ is obtained at the output. Similarly, resistance $R_{ON,PM}$ is the result of connection (b) where only relay 1 and relay 4 are in *on* state. In the case of connection (c), the output is $R_{OP,NM}$ and all relays are in *on* state. Finally, connection (d) is configured when relay 2 and relay 3 are in the *on* state and the obtained output is resistance $R_{MP,NO}$.

Figure 4 displays the flow chart of measurement process and control program to identify the resistance value according to the VDP method. The control program uses LabVIEW platform which makes the setup fully automatic with the facility of real time analysis and data plotting. Also, the setup has provision to check the conductivity between probe-tips and metal contact pads in order to ensure the Ohmic behavior prior to the actual resistance measurement. The program begins with setting the source current (I_s) and subsequently applying it to the DUT. For proper measurement, we have fixed the voltage measuring range (V_R) from 1 V to 5 V because the DUT resistance and the source current are both varying quantities. Therefore, if the calculated voltage (V_m) falls in the measuring range, then the resistance measurement process will initiate; otherwise, I_s will be doubled for V_m smaller than V_R and halved for V_m higher than V_R. In the sequence of resistance measurement, the switching network is activated for connection 1 and the resistance $R_{MN,PO}$ is measured. Similarly, the switching network is configured for the remaining configurations and the resistances $R_{ON,PM}$, $R_{OP,NM}$, and $R_{MP,NO}$ are measured. Further, after taking an average of symmetric resistance values, the VDP mathematical equation (1) is applied to obtain the resistance of the DUT. For the temperature dependent resistance measurement, again this process is repeated to identify the resistance of the DUT at a particular temperature. The measurement process is designed such that the effect of parasitic capacitance should be minimal. The *RC* time constant of the electrical setup is in the range of few seconds due to high resistance and large capacitance of the sample. Therefore, after sourcing the current at one side of the sample, the setup waits approximately 15 s until voltage saturates and parasitic capacitance is charged.[19]

Figure 5(a) represents the calibration results of this setup. We have used a network of four resistors based on the literature[20] to calibrate the developed setup for the square van der Pauw sample. Four probe resistance values with the corresponding source current for a resistor starting from 10 Ω to 10 MΩ have been displayed in Fig. 5(a). It can be seen that experimental values (symbol) shows good agreement with the standard four-resistor model[20] (line). Furthermore, similar measurement has been performed with as-deposited phase change materials such as GST, AIST, and IST to confirm the measurement accuracy in the high resistance regime. Importantly, the obtained resistance values are also inline with the four-resistor-model[20] validating the measurement capability of the setup in high resistance range. Moreover, the calculated resistivity of as-deposited GST, AIST, and IST is 0.6 Ω m, 3 Ω m, and 1000 Ω m, respectively, and it is found to be in good agreement with the previous reports.[23,24] The developed temperature dependent resistance measurement setup is employed to identify the crystallization temperature of phase change materials. Figure 5(b) represents the temperature dependent resistivity plot of 100 nm thick GST, AIST, and IST samples obtained from the developed setup. Starting from the

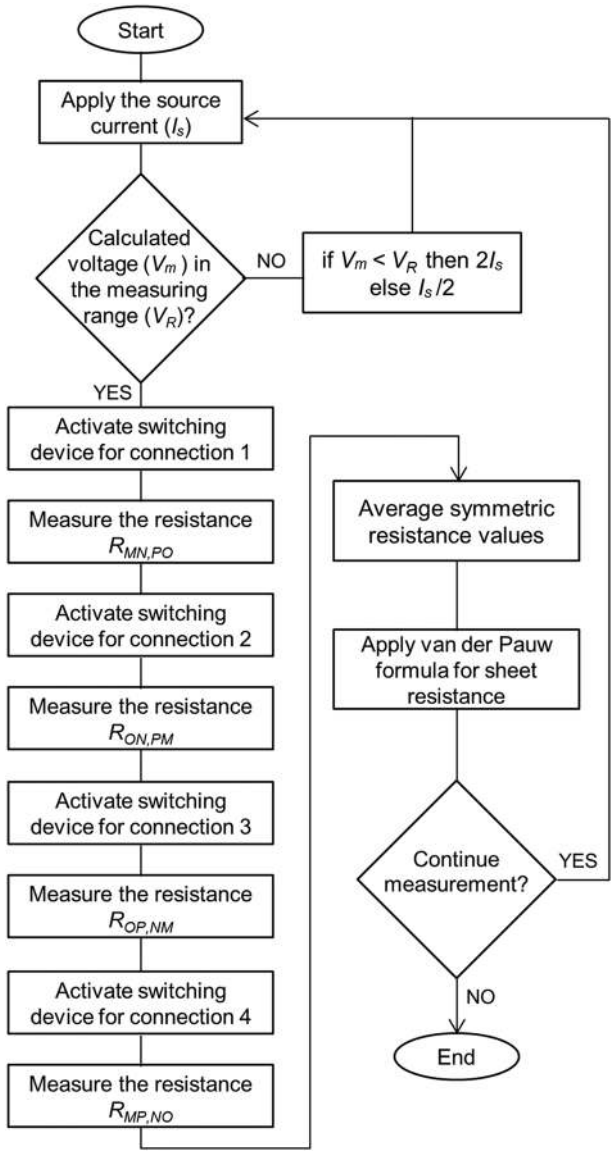

FIG. 4. Flowchart of the program to calculate the resistance as per the VDP method.

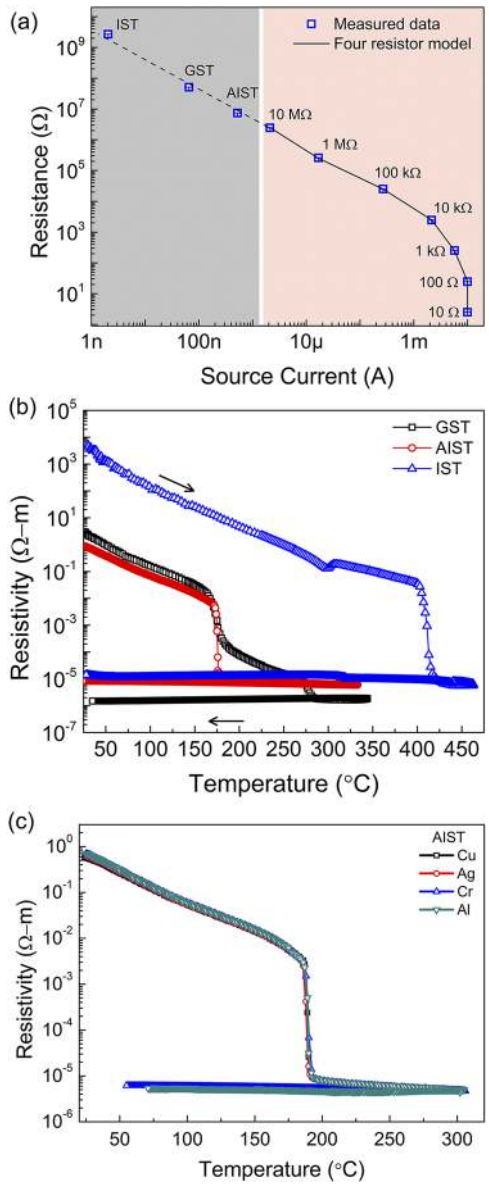

FIG. 5. (a) The calculated resistance values using the four-resistor model[20] and experimental data (symbol) and their fitting (line) for calibration of the setup. (b) Temperature dependent resistance of GST, AIST, and IST exhibits amorphous to crystalline phase transitions by means of rapid change in resistance during amorphous to crystalline phase transformation. (c) Resistivity measurement of AIST upon temperature using different metal contacts.

as-deposited amorphous phase, both materials show the gradual change in resistance with temperature due to semiconducting behavior. For GST, larger change in resistance is identified at 160 °C due to amorphous to cubic phase transformation and further cubic to hexagonal phase change is observed at 290 °C. AIST displays the rapid change in resistance due to amorphous to hexagonal phase transition at 170 °C. Crystallization temperatures obtained for GST and AIST with the developed setup are in line with the previous reports.[20,21] The as-deposited amorphous IST sample shows the high resistance of ∼10 GΩ at room temperature. Similar to GST and AIST, gradual change in resistance is observed upon increasing the temperature for IST also. Interestingly, IST shows higher crystallization temperature of 300 °C with the current setup which is well matched with other measurement techniques.[22,23]

Figure 5(c) demonstrates the temperature dependent resistivity measurement of AIST materials using different metal contacts such as Ag, Cu, Al, and Cr which confirms the effect of contact resistance for various elements with DUT. No significant change in resistivity and crystallization temperature is observed during measurement.

IV. CONCLUSION

The temperature-dependent resistance measurement setup with a custom-built SNB is developed based on the VDP method, which can measure the resistance from few mΩ to 10 GΩ. A detailed description of the setup and measurement strategy has been discussed. A custom-built SNB is designed to switch source and sense terminals across the sample with the characteristics to provide the minimum possible leakage current and capacitance in the circuit. Furthermore, this setup demonstrated the capability of determining the source current automatically from few nA to 10 mA according to the nature of DUT. Also, this setup offers a low cost, LabVIEW controlled user friendly simple and robust design by combining high precision electronic components in the SNB, which operates based on the algorithm of the van der Pauw method. Calibration and experimentation of the setup has been demonstrated using some of the chalcogenide based semiconducting phase change thin films (GST, AIST, and IST). The obtained experimental results validate phase transitions, as evidenced by rapid change in resistances during amorphous to crystalline phase transformation. Moreover, the developed setup could also be useful in various scientific and industrial applications with different samples including semiconductors, metals, and insulators.

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