Control Schemes for Equalization of Capacitor Voltages in Neutral Clamped Shunt Compensator

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***Abstract*—Voltage imbalance in capacitors is a well-known problem in compensator topologies which use two or more capacitors. This imbalance may exist even if the load does not contain any dc component, due to practical factors. However, when the load contains a dc part, the voltage imbalance problem becomes critical. In this paper, a two-quadrant chopper has been used to regulate the capacitor voltages in a two-capacitor compensator structure. Two different control strategies for the two-quadrant chopper to equalize the voltage of the capacitors have been proposed. The strategies are validated through detailed simulation studies. Experiments have also been carried out to validate the hysteresis control of chopper.**

***Index Terms*—Active shunt compensators, chopper control, dc load, voltage equalization, voltage imbalance.**

I. Introduction

A shunt compensator suitable for a three-phase, four-wire distribution system [1] is shown in Fig. 1. The compensator uses a current source, comprising of a voltage source inverter (VSI) with six switches $(S_1 - S_6)$, operated in a hysteresis band current control scheme. It has two capacitors whose common terminal is the neutral point of the compensator. The switches $S_7 - S_8$ and the inductor L_{ch} form a chopper which is used to equalize the capacitor voltages. The resistor R_{ch} arises due to the finite quality factor of the inductor. The compensator is directly coupled to the ac system through the interface inductor L that has a resistance of R as well.

The neutral points of the source, the load, and the compensator are connected together as shown in Fig. 1. If the loads connected to the system draw significant dc current, the use of a coupling transformer prevents the compensation of the zero sequence current. Therefore, the compensator structure given in [2] is not suitable for such loads. The compensator given in [3] uses a coupling transformer, which may be discarded for a low voltage distribution system. The compensator then is similar to that shown in Fig. 1, except that it does not include the chopper circuit.

The compensator topology of Fig. 1 may employ more than two capacitors when four or higher level inverters are used. Unfortunately, however, the capacitors in such compensator topologies are associated with the problem of voltage imbalance [4]–[7]. This problem may be classified into two categories—minor and major voltage imbalance. The minor voltage imbalance problem arises due to practical factors when

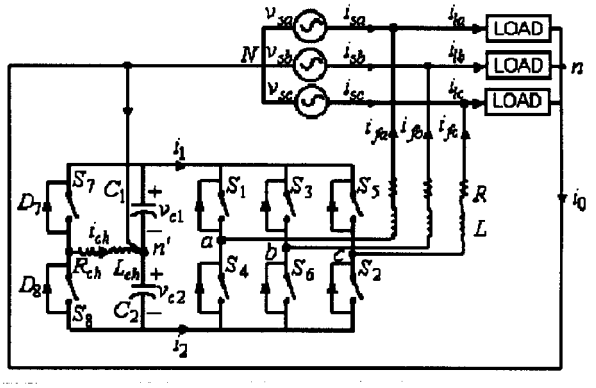

Fig. 1. Compensator for star-connected three-phase, four-wire distribution system.

the load does not have a dc component. The following practical factors are responsible for small imbalance in the capacitor voltages [7], [8]

- unequal capacitance leakage currents;
- unequal delays in the semiconductor devices;
- asymmetrical charging of the capacitors during transients;
- asymmetrical circuit configuration (due to measurement and signal conditioning circuit).

The minor voltage imbalance problem has been discussed in [4]–[7]. These references also provide guidelines for the remedial actions that can be taken to alleviate this problem, such as changing the switching instants (of gating signals S_1 to S_6 in Fig. 1) in a direct or indirect manner so as to achieve the voltage balance.

However, when the load current contains a dc component, the capacitors are associated with the major voltage imbalance. For this case, the methods suggested in [5]–[8] will fail to deliver due to the limit imposed on the switching rate. Beyond that limit, the tracking of the reference current will be affected. The major voltage imbalance problem of capacitors has been dealt with in [1]. However, in this control strategy, the maximum chopper current is not constrained. Therefore, the device implementing the chopper switch must have sufficiently high current rating. In this paper, we propose two control schemes of chopper—duty cycle control and hysteresis band current control which do not suffer from the mentioned limitation.

II. Compensator Structure

The VSI is operated in a hysteresis band current control to track the reference currents i^*_{fa}, i^*_{fb}, and i^*_{fc} in phases a, b, and

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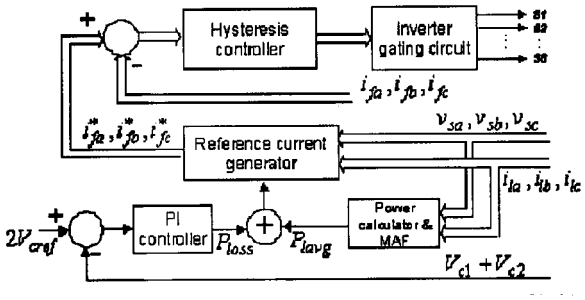

Fig. 2. Control scheme for VSI operating as current source.

c, respectively. The control scheme for the VSI operating as a current source is shown in Fig. 2. The reference currents are generated on the basis of the theory of instantaneous symmetrical components [2], [9] and these currents are given by

$$i_{fa}^{*} = i_{la} - \frac{v_{sa} + \beta\,(v_{sb} - v_{sc})}{\sum_{i=a,b,c} v_{si}^{2}}\,(P_{lavg} + P_{loss}) \quad (1a)$$

$$i_{fb}^{*} = i_{lb} - \frac{v_{sb} + \beta\,(v_{sc} - v_{sa})}{\sum_{i=a,b,c} v_{si}^{2}}\,(P_{lavg} + P_{loss}) \quad (1b)$$

$$i_{fc}^{*} = i_{lc} - \frac{v_{sc} + \beta\,(v_{sa} - v_{sb})}{\sum_{i=a,b,c} v_{si}^{2}}\,(P_{lavg} + P_{loss}) \quad (1c)$$

where $\beta = \tan\phi/\sqrt{3}$. ϕ is the desired phase angle. between the supply voltages v_{sa}, v_{sb}, and v_{sc} and the line currents i_{sa}, i_{sb}, and i_{sc}, respectively. Note that for unity power factor operation $\phi = 0$, and therefore, $\beta = 0$. The term P_{lavg} is the dc value of the load power and is computed using a moving average filter (MAF) that has an averaging time of half a cycle. The term P_{loss} in (1) accounts for the losses in the inverter. To generate P_{loss}, a feedback loop is used, which regulates the total voltage $v_c = v_{c1} + v_{c2}$ across the two capacitors to a constant value $2V_{cref}$ as shown in Fig. 2.

III. State Space Model of Inverter-Chopper

The actual filter currents i_{fa}, i_{fb}, and i_{fc} in Fig. 2, the capacitor voltages v_{c1} and v_{c2}, and the chopper current i_{ch} are obtained using the state space model of combined inverter chopper [1] of Fig. 1. In brief, the state space model is

$$\frac{d}{dt}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} u \quad (2)$$

where

$$x_1 = [i_{fa} \quad i_{fb} \quad i_{fc}]^t,$$

$$x_2 = [v_{cl} \quad v_{c2} \quad i_{ch}]^t,\ u = [v_{sa} \quad v_{sb} \quad v_{sc}]^t \quad \text{and}$$

$$A_{11} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R}{L} \end{bmatrix} \quad A_{12} = \begin{bmatrix} \frac{S_a}{L} & -\frac{\overline{S}_a}{L} & 0 \\ \frac{S_b}{L} & -\frac{\overline{S}_b}{L} & 0 \\ \frac{S_c}{L} & -\frac{\overline{S}_c}{L} & 0 \end{bmatrix}$$

$$A_{21} = \begin{bmatrix} -\frac{S_a}{C} & -\frac{S_b}{C} & -\frac{S_c}{C} \\ \frac{\overline{S}_a}{C} & \frac{\overline{S}_b}{C} & \frac{\overline{S}_c}{C} \\ 0 & 0 & 0 \end{bmatrix}$$

$$A_{22} = \begin{bmatrix} 0 & 0 & -\frac{P_{13}}{C} \\ 0 & 0 & -\frac{P_{23}}{C} \\ \frac{P_{13}}{L_{ch}} & -\frac{P_{23}}{L_{ch}} & -\frac{R_{ch}}{L_{ch}} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} -\frac{1}{L} & 0 & 0 \\ 0 & -\frac{1}{L} & 0 \\ 0 & 0 & -\frac{1}{L} \end{bmatrix} \quad B_2 = [0]_{3\times 3}.$$

Note that S_a, $\overline{S}_a$, S_b, $\overline{S}_b$, S_c, $\overline{S}_c$, S_u, and S_l represent gating signals for switches S_1, S_4, S_3, S_6, S_5, S_2, S_7, and S_8, respectively. For example, $S_a = 1$ implies that S_1 is closed, and $S_a = 0$ implies that S_1 is open. A gating signal for S_4 is the complementary signal $\overline{S}_a$. P_{13} and P_{23} are binary variables and are given by

$$P_{13} = \overline{S}_l \bullet \left\{S_u + (\overline{sign} \bullet mag)\right\} \quad (3)$$

$$P_{23} = \overline{S}_u \bullet \left\{S_l + (sign \bullet mag)\right\}. \quad (4)$$

Here, the symbol $\bullet$ and $+$ are logical AND and OR operators, respectively. In logical expressions, the terms in (3) and (4) are explained as

$$sign = \begin{cases} 1 & for\ i_{ch} > 0 \\ 0 & for\ i_{ch} \le 0 \end{cases},\ mag = \begin{cases} 1 & for |i_{ch}| > 0 \\ 0 & for |i_{ch}| = 0 \end{cases}. \quad (5)$$

IV. Voltage Imbalance in Capacitors

The voltage imbalance problem of the capacitors C_1 and C_2 of the compensator (Fig. 1) is discussed in [1]. In this topology, if the load currents contain dc components, one capacitor gets charged and another gets discharged. When the compensator is working perfectly, the current i_0 (Fig. 1) flows through the path $n - n'$, and $i_{sa} + i_{sb} + i_{sc} = 0$. Considering all kinds of unbalances in the load and steady state operation, current i_0 can be assumed to be a nonsinusoidal periodic waveform. In general, the spectrum of i_0 may contain a dc component, supply frequency component, and its harmonics, that is

$$i_o = i_{la} + i_{lb} + i_{lc} = I_o + \sum_{h=1,2,3\ldots}^{\infty} I_h \sin h(\omega t + \phi_h). \quad (6)$$

The second term on the right-hand side of (6) is responsible for generating ripples in the capacitor voltages at fundamental and harmonic frequencies. For large values of capacitors, these ripples are small and do not cause any problems. However, the effect of the first term I_0, which is the dc part of i_0, is significant as it is directly responsible for causing the voltage imbalance. A feedback loop regulates the sum of the capacitor voltages $v_{c1} + v_{c2}$ to be a constant $2V_{cref}$. Consequently, current i_0 divides equally between the two capacitors. Therefore, we can write

$$v_{c1} \approx V_{c1} = V_{c10} - \frac{I_o}{2\,C}t \quad (7a)$$

$$v_{c2} \approx V_{c2} = V_{c20} + \frac{I_o}{2\,C}t \quad (7b)$$

where t is the time in seconds and V_{c1} and V_{c2} are the average values of v_{c1} and v_{c2}, respectively. At $t = 0$, $v_{c1} = V_{c10}$ and $v_{c2} = V_{c20}$. In general, V_{c10} and $V_{c20} \neq V_{cref}$. Thus, the capacitors may have unequal initial voltages and voltage drift due

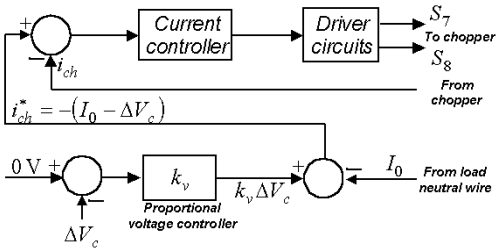

Fig. 3. Schematic of chopper control.

to I_0. It is also clear that if I_0 is sufficiently large, in a few cycles V_{c1} or V_{c2} will go below the peak of the system ac voltage and the tracking of reference filter currents will be lost. If I_0 is small, it will lead to imbalance after several cycles. Hence, it is necessary to regulate the voltage of each capacitor to a reference value (V_{cref}), when three phase load draws a dc current. In the present work, a two-quadrant chopper has been employed to regulate the voltages of each capacitor. Two control schemes have been discussed. In principle, the chopper is required in the steady state to generate a current i_{ch}, whose average value (I_{ch}) is equal and opposite to the average value of i_0. Effectively, it means that the current I_o is bypassed around the capacitors C_1 and C_2, through switches $S_7 - D_7$ and $S_8 - D_8$.

V. Control Schemes of Chopper

In [1], the problem of voltage imbalance has been corrected by a single cycle control of the chopper using the state space model. This uses an approximation in which the currents i_1 and i_2 (Fig. 1) are ignored due to fast action of the chopper. However, this method has the disadvantage that the peak chopper current is large. To overcome this problem, a new control scheme is proposed.

The block diagram of chopper control is shown in Fig. 3. It incorporates an outer voltage control loop and an inner current control loop. The current i_0 in the load neutral path $n - n'$ is sensed and filtered to remove the fundamental and the harmonics, thus leaving only I_0 (the average value of i_0). The difference in capacitors voltage $v_{c1} - v_{c2}$ is sensed and filtered to remove the ripples. The filtered voltage difference is denoted as $\Delta V_c = V_{c1} - V_{c2}$. The proportional voltage controller outputs a control signal $k_v \Delta V_c$ which is added with $-I_0$ to generate the reference chopper current i_{ch}^*. The inner control loop ensures that the average chopper current is equal to i_{ch}^*. The current control loop has faster dynamics than the voltage control loop. The reference current for the chopper can be written as

$$i_{ch}^* = -(I_o - k_v \Delta V_c). \tag{8}$$

An error e is formed using the reference chopper current as per (8) and the actual chopper current i_{ch}

$$e = i_{ch}^* - i_{ch}. \tag{9}$$

The current controller (Fig. 3) can be a hysteresis controller or a PI controller. In the following subsections, these two chopper control schemes to equalize the voltages of the capacitors will be discussed.

A. PI Duty Cycle Control

In this method, the chopper is run at fixed frequency, which is sufficiently high so that i_{ch} is essentially ripple free. The current controller in Fig. 3 is a PI controller. The duty cycle is limited between 0 and D_{max} and is determined as follows:

$$D = K_p\, e + K_i \int e\, dt \tag{10}$$

where K_p and K_i are proportional and integral constants of the PI controller. The steady state value of D is approximately 0.5 for a high Q inductor. The value of D_{max} is always chosen to be higher than 0.5. Its value decides the maximum chopper current and the transient response of the loop. It is chosen to be 0.7 in the simulation.

Depending upon the polarity of ΔV_c, a particular switch of the chopper S_7 or S_8 is operated. If ΔV_c is less than or equal to zero, then the switch S_8 is operated at the duty cycle given by (10). On the other hand, if ΔV_c is greater than zero, then the switch S_7 is operated at the duty cycle given by (10).

B. Chopper Current Control in Hysteresis Band

In this control scheme, the chopper circuit is employed to track i_{ch}^* in a hysteresis band. This nullifies the initial voltage imbalance in the capacitors as well as the voltage drift due to the dc component of the load current. As compared to the single cycle control [1], this method has the advantage that i_{ch} is limited to a value close to $-I_0$ in the steady state. In case of single cycle control [1], i_{ch} may reach three or four times to that of I_0, and thus, the switching devices and inductor need to be over-rated.

In hysteresis control mode, the switches S_7 and S_8 (Fig. 1) operated at high frequency. Therefore, the switching losses in the hysteresis control associated with these switches are higher than those in the PI duty cycle control, in which only one chopper switch is operated at a time. However, the implementation of the hysteresis control scheme is easier than that of the PI duty cycle control scheme.

VI. Simulation Results

In this section, the system of Fig. 1 has been simulated using MATLAB 5.3. The source voltages are assumed to balanced and sinusoidal. The load consists of (i) an unbalanced three-phase resistive load; and (ii) a three-phase half bridge diode rectifier with highly inductive load. The load currents are shown in Fig. 4. The system parameters are as follows:

$$\begin{aligned} v_{sa} &= 440\sqrt{\frac{2}{3}} \sin 100\pi t \\ C_1 &= C_2 = 2200\,\mu F,\ R = 2\Omega,\ L = 20\ \text{mH} \\ K_p &= 10,\ K_i = 1,\ V_{cref} = 500\ \text{V} \\ L_{ch} &= 200\text{mH},\ R_{ch} = 2\Omega. \end{aligned}$$

Injected filter current hysteresis band of 1 A and chopper current hysteresis band of 0.2 A are chosen.

From the given source voltages and the load currents, the reference currents i_{fa}^*, i_{fb}^*, and i_{fc}^* are generated using (1a)–(1c). In this algorithm, β is set to 0 for unity power factor operation.

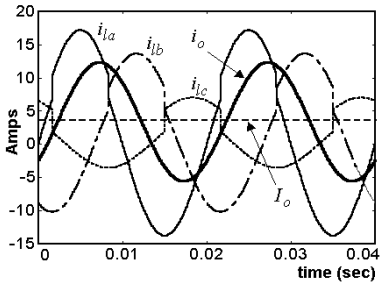

Fig. 4. Load currents with dc component.

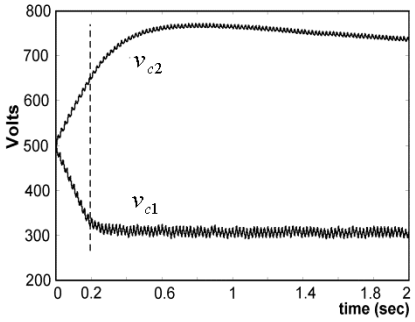

Fig. 5. Voltage imbalance in capacitors.

The term P_{lavg} in (1a)–(1c) is computed using moving average filter [2] over half cycle. The P_{loss} term is computed using PI controller (Fig. 2), with K_p and K_i as given before. The P_{loss} term is updated once in a cycle. The state space model of the inverter-chopper given in Section III has been used to compute the actual filter currents, capacitor voltages, and chopper current. Once we know the actual and the reference filter currents, the VSI is operated in order to track them in the hysteresis band (1 A). If there is a dc component in the load, the chopper operates to eliminate the voltage imbalance in capacitors as per control schemes, described in Section IV (Fig. 3).

A. Operation without Chopper

In this simulation, the switches S_7 and S_8 are assumed to be off. It is seen from Fig. 4 that average value of neutral current $I_0 = 3.4$ A. The effect of this dc component is to discharge and charge the capacitors C_1 and C_2, respectively, as explained in Section IV. The effect on the voltage of the capacitors and the tracking performance is shown in Figs. 5 and 6, respectively.

Due to the presence of a positive I_0 (Fig. 4), v_{c1} decreases and v_{c2} increases continuously as per (7a) and (7b). However, (7a) and (7b) remain valid only until the current tracking is faithful. It is observed that beyond ten cycles (i.e., $t = 0.2$ s), the voltages v_{c1} and v_{c2} (Fig. 5) do not decrease and increase at the same rate. After $t = 0.2$ s, v_{c1} becomes constant and the tracking does not remain faithful. As a consequence of the loss of tracking, the voltages v_{c1} and v_{c2} stabilize to 300 and 700 V, respectively, after the 100th cycle (Fig. 5), instead of the reference value of 500 V.

Fig. 6 shows the steady state tracking performance over one cycle of the supply voltage. To compare the nature of the voltage and current waveforms in the same graph, the voltages in Fig. 6 have been scaled down by 50. From Fig. 6, it is observed that between the points p and q, the tracking is lost as voltage; v_{c1} is close to the source voltage v_{sa}. As a consequence of this, the compensator is unable to track the sudden changes in the reference current (i^*_{fa}) at the points p and q. It is observed that between the points r and s, v_{c1} is less than v_{sa}, and therefore, the current i_{fa} has negative slope. Later, after the point q, v_{sa} is smaller than v_{c1}, and therefore, the tracking is regained for the rest of the voltage cycle. In summary, the operation without chopper results in highly unequal capacitor voltages (300 and 700 V) and distorted filter currents resulting in imperfect compensation.

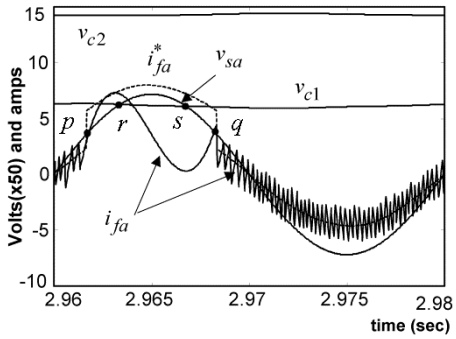

Fig. 6. Effect of dc component of load on tracking performance.

B. Operation with Chopper

In this section, the chopper operation under two control strategies has been simulated. An initial voltage imbalance of $\pm$ 150 V has been assumed in each case, giving $\Delta V_c = 300$ V.

1) Duty cycle control: In this method, the chopper is operated at a frequency of 1800 Hz. Equations (8)–(10) and the chopper current computed from the state space model are used to calculate the duty cycle D. The capacitor voltages and chopper currents are shown in Figs. (7a) and (7b), respectively. It is seen that the chopper is able to cancel the initial voltage imbalance and maintain the capacitor voltages at the reference value of 500 V. As a result, the compensator is able to provide the unity power factor operation.

2) Hysteresis band current control: In this control scheme, the switches S_7 and S_8 are controlled in such a way that the chopper circuit tracks $-(I_0 - k_v \Delta V_c)$. This counteracts the initial voltage imbalance in the capacitors and nullifies the effect of I_0 on the capacitor voltages in the steady state. The simulation results are shown in Fig. (8a) and Fig. (8b). From Fig. (8a), it is seen that with the hysteresis controller, both the voltages v_{c1} and v_{c2} are stabilized to the reference value of 500 V with a small ripple. Fig. (8b) shows that the chopper current i_{ch} tracks the reference value $-(I_0 - k_v \Delta V_c)$ with a hysteresis band of $\pm$ 0.2A. For this hysteresis band and the chopper circuit parameters given in Section VI, the chopper switching frequency is approximately 3 kHz in the steady state.

C. Current Rating of the Chopper

If the frequency of the chopper is sufficiently high such that i_{ch} is nearly ripple free, then the chopper current rating is at least i_{0max}. An additional current rating is required to provide the component $k_v \Delta V_c$ of the chopper current, to correct any initial voltage unbalance at the time when the chopper starts working.

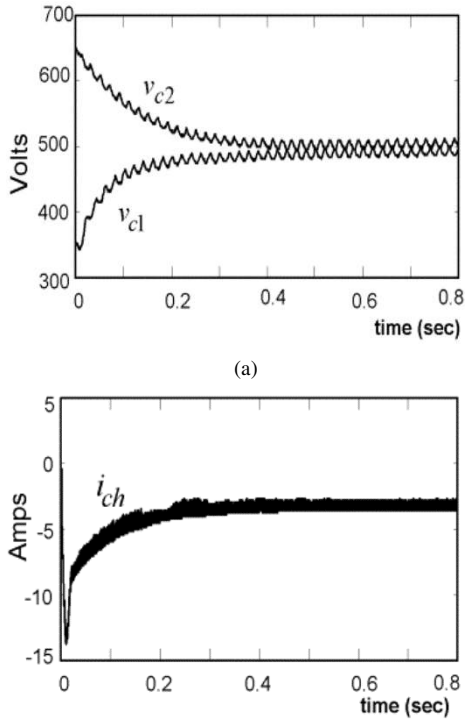

Fig. 7. (a) Capacitor voltages with chopper duty cycle control. (b) Chopper current using duty cycle control.

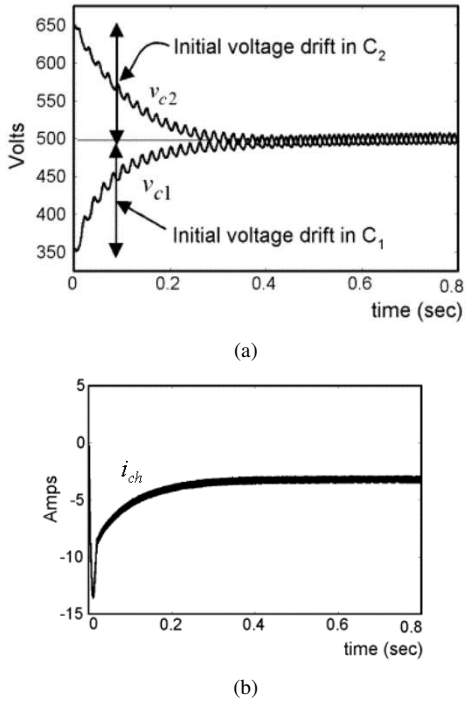

Fig. 8. (a) Capacitor voltages with chopper hysteresis control. (b) Chopper current using hysteresis control.

Under dc load condition, when the chopper is not turned on, one of the capacitor voltages settles around the peak of the system phase voltage v_{peak}. The other capacitor will have a voltage of $2V_{cref} - v_{peak}$. Therefore, in the worst case, the current rating of the chopper should be approximately $2k_v(V_{cref} - v_{peak}) + i_{0max}$. For example, in simulation V_{cref} and v_{peak} are taken as

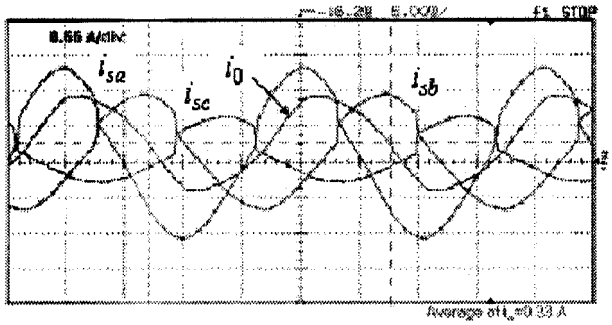

Fig. 9. Experimental load currents.

500 V and 360 V, respectively. For $k_v = 0.02$, the current rating of the chopper is found to be approximately 18 A. It is seen from the simulation results of Figs. (7b) and (8b) that the peak chopper current is 15 A, which compares well with the worst case value calculated before.

VII. Experimental Results

A scaled down prototype with voltages reduced by a factor of ten has been chosen for experimentation. The source voltages are balanced and sinusoidal with a peak of 36 V. The system voltages v_{sa}, v_{sb}, and v_{sc} and load current i_{la}, i_{lb}, and i_{lc} are sensed using hall effect voltage and current sensors. The voltage and current signals are acquired by a PC (P-II, 350 MHz) through two data acquisition cards (9118 DG NuDAQ). The algorithm for the generation of the reference filter currents is implemented in Turbo C. To obtain the average load power P_{lavg}, a moving average filter has been used. Then, the filter reference currents are generated using (1a)–(1c). This computation takes approximately 100 μ s. This speed is sufficient to generate filter currents containing harmonics up to 1 kHz through a VSI-based current source using the hysteresis control.

The steady state load currents are shown in Fig. 9. As seen from Fig. 9, the load currents are unbalanced ac due to unequal resistive loads of 25, 35, and 100 Ω in phases a, b, and c, respectively. In addition, there is a dc component due to the three-phase half wave rectifier. The total dc component of the neutral current I_0 shown by the dotted line in Fig. 9 is 0.33 A.

A. Operation without Chopper

Initially, the load is unbalanced resistors only, and therefore, the voltages of the capacitors C_1 and C_2 are regulated to 50 V, which is above the peak system voltage of 36 V. The rectifier containing dc is switched on at the instant t_1 as shown in Fig. 10. Due to the action of the dc component of neutral current I_0, the capacitor C_1 is discharged, while the capacitor C_2 is charged until v_{c1} settles at a little below the peak of the system voltage (approximately 25 V). However, the PI voltage control loop of inverter ($Kp = 0.3$, $Ki = 0.001$) maintains the total capacitor voltage $(v_{c1} + v_{c2})$ at 100 V. The tracking current performance of the compensator in phase a is shown in Fig. 11. It is seen in Fig. 11, that the tracking is lost between the points p and q, because v_{c1} is close to system voltage v_{sa}. Between the points r and s, the slope of i_{fa} is negative due to the fact that v_{c1} is

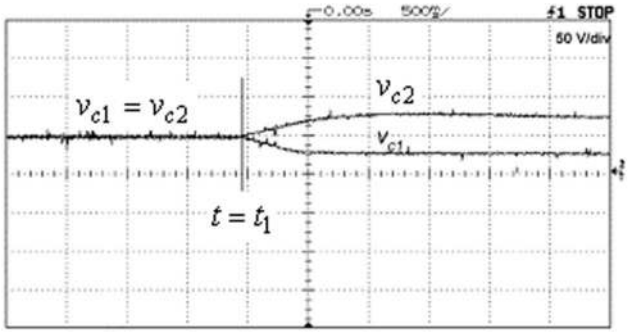

Fig. 10. Voltage imbalance in capacitors: experimental.

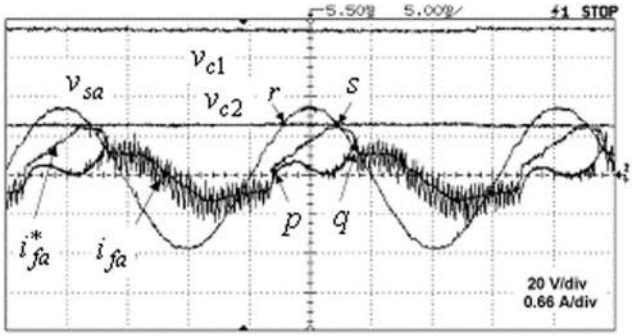

Fig. 11. Effect of dc load on tracking performance: experimental.

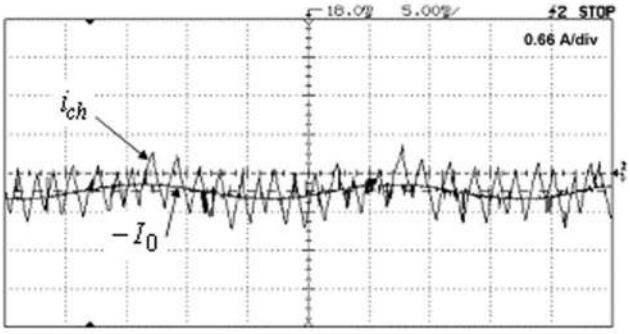

Fig. 12. Chopper current using hysteresis control: Experimental.

a little below v_{sa}. The experimental waveforms of Fig. 11 are similar to the simulated waveforms given in Fig. 6.

B. Operation with Chopper

In this experiment, the compensator is operated first without chopper as discussed before. The chopper is then turned on and operated using hysteresis band current control (Section V, Part B) which is tracking $-(I_0 - k_v \Delta V_c)$. Active lowpass filters with cutoff frequency of 10 Hz are used to obtain I_0 from the signal i_0 and ΔV_c from v_{c1} and v_{c2}. In the experiment, the value of k_v is chosen as 0.001. In the steady state, ΔV_c tends to zero and the chopper effectively tracks $-I_0$ to maintain equal capacitor voltages. This is shown in Fig. 12, which displays the waveforms of $-I_0$ and i_{ch}. It can also be seen from this figure that the switching frequency of the chopper, as observed from waveform of i_{ch}, is approximately 500 Hz. This relatively low switching frequency is due to a large hysteresis band. Fig. 13

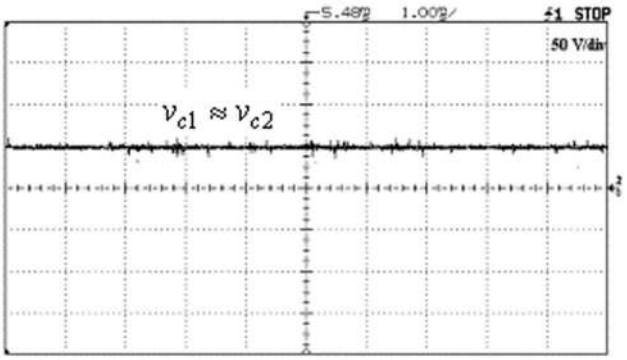

Fig. 13. Equalized voltage due to chopper action.

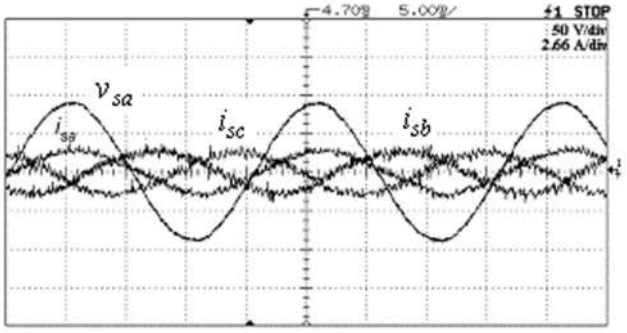

Fig. 14. Compensated source currents.

shows that the capacitor voltages v_{c1} and v_{c2} are equalized close to the reference value of 50 V each due to the chopper action. This ensures a good tracking performance of the inverter. The resulting compensated source currents are shown in Fig. 14. It is seen that the source currents after compensation are balanced and sinusoidal and are in phase with their respective phase voltages. The chopper is thus able to nullify the effect of the dc component of the neutral current in the steady state.

VIII. Conclusions

A shunt compensator topology with two capacitors and inverter-chopper has been analyzed. A state space model of the system has been given. The problem of voltage imbalance arises in the case of load currents containing dc components. A control strategy for chopper employing an inner current and an outer voltage loop has been proposed for eliminating the voltage imbalance. Simulation results using a state space model are given for both the PI duty cycle and the hysteresis control of the chopper. The hysteresis control has been further verified by experiments for loads containing three-phase unbalanced resistance and three-phase half bridge rectifier. The effectiveness of the proposed control strategy has been demonstrated.

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