Analysis of High-Frequency Measurement of Transistors Along With Electromagnetic and SPICE Cosimulation

Sebastien Fregonese, Marco Cabbia, Chandan Yadav, Marina Deng, Soumya Ranjan Panda, Magali De Matos, Didier Celi, Anjan Chakravorty, Thomas Zimmer

Analysis of high frequency measurement of transistors along with electromagnetic and SPICE co-simulation

Sebastien Fregonese, Marco Cabbia, Chandan Yadav, Marina Deng, *IEEE member,* Soumya Ranjan Panda, Magali De Matos, Didier Céli, Anjan Chakravorty, and Thomas Zimmer, Senior *Member, IEEE*

Abstract—THz silicon based electronics is undergoing rapid developments. In order to keep this momentum high, an accurate and optimized on-wafer characterization procedure needs to be developed. While evaluating passive elements, the measured s-parameter data can be verified by a direct use of EM simulation tools. However, this verification requires to precisely introduce part of the measurement environment such as the probes, the pads and access lines to accurately predict the impact of calibration and layout for on-wafer measurements. Unfortunately, this procedure is limited to passive elements. Hence, in this work, we propose a new procedure to emulate the measurement of active devices using an electromagnetic-SPICE co-simulation. By this method, one can clearly highlight that a measurement artefact that was observed for the transistor measurement can be reproduced. One of the most representative example of measurement artefact involves the measurement and estimation of f_{MAX} which is not constant over all frequency band. Also the measurement is difficult to perform above 40 GHz. This typical problem is now undoubtedly attributed to the probe-to-substrate coupling and probe-to-probe coupling which are strongly dependent on the probe geometry. Finally, this co-simulation procedure evidently underlines the need for an optimized de-embedding procedure above 200 GHz.

Index Terms—On-wafer, s-parameter measurement, HBT, MOSFET, HEMT, high frequency, millimeter-wave, THz, EM simulation, calibration, probes, compact model, f_{MAX}, HICUM, de-embedding, TRL.

I. INTRODUCTION

THE THz based silicon electronics has been under development for about fifteen years and has undergone a rapid acceleration in the last five years. Its main advantages include its moderate cost compared to that of the III-V technologies for large market volume [1] and its capability to integrate different parts of the system such as THz sensor, frequency mixer, etc., and digital information processing unit within a single chip removing the complexity of packaging different modules required in more conventional THz technologies [20].

Furthermore, the competitive and rapid development of a silicon based THz system requires accurate CAD software with advanced capabilities such as a EM-Spice approach. These CAD models involve calibrated models from DC and high frequency measurements. Hence it is of utmost importance to understand the transistor s-parameters measurement results and subsequently to verify the validity of the model in the upper frequency range, i. e. above 40 GHz. One of the most typical examples that highlights the complexity of the measurement is the shape of frequency dependent unilateral power gain (U) plot that theoretically drops with -20 dB/dec [2] and thus the maximum oscillation frequency (f_{MAX}) can be obtained through the constant gain x bandwidth product assumption. For example, Fig. 1 (from [3]) depicts the f_{MAX} determination of the same device measured at two different laboratories showing two different results with two different trends above 40 GHz. Unfortunately high frequency measurement on silicon technology is still a challenge even above 40 GHz when analyzing sensitive parameters such as f_{MAX}. This is due to numerous uncertainties and inaccuracies [4]–[7] summarized below. This problem is strongly increased at higher frequency.

First, on-wafer TRL calibration is commonly admitted as a reference method for high frequency measurement since the reference plane is well defined and because the probe environment does not change between calibration and measurement (calibration standards and DUTs are on the same substrate). Unfortunately, it imposes the shift of one of the two probes to measure the line. This can induce discrepancies in probe positioning [5], [8], [9], especially when a manual probe positioner is used.

Second, the pad layout design combined with the probe geometry can strongly influence the probe-to-substrate coupling as demonstrated in [10]. Also, we have shown, by employing a specific EM probe model for each of the frequency bands (WR2.2 (325-500 GHz), WR3.4 (220-325 GHz), WR5 (140-220 GHz)) that each probe has a specific geometry enabling a different EM field confinement that entails a

Sebastien Fregonese, Marco Cabbia, Soumya Ranjan Panda, Marina Deng, Magali De Matos, and Thomas Zimmer are with the IMS Laboratory, University of Bordeaux France (e-mail: sebastien.fregonese@ims-bordeaux.fr).

Chandan Yadav Yadav is now working with NIT Calicut, India. Earlier he was associated with IMS laboratory, University of Bordeaux, France

Didier Céli is with STMicroelectronics, Crolles, France.

Soumya Ranjan Panda and Anjan Chakravorty are with IIT Madras, India.

different substrate-to-probe coupling. This can lead to erroneous trends and results in inaccurate s-parameter measurements.

Third, different research labs [11], [12], [13] [5] have shown that measurement results can be influenced by the adjacent structures, resulting in erroneous s-parameters. On the other hand, advanced technologies have a high cost per square millimeter which imposes to increase the density of the test structures for device compact modelling. Hence, a problematic trade-off appears between the cost and measurement accuracy.

Finally, the conventional de-embedding procedure is based on lumped elements approach. Hence, the validity range of de-embedding is evidently a function of frequency and structure size. Please note that although more complex approaches have been proposed, they are still not widespread [6], [14], [15].
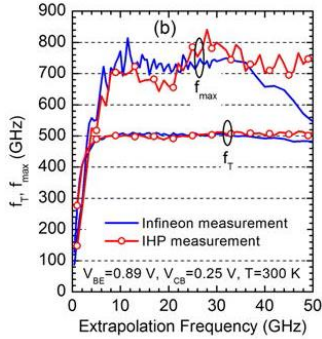

Fig. 1: Dependence of f_T and f_{MAX} on extrapolation frequency for the same HBT measured at IHP and Infineon. SOLT calibration with an impedance standard substrate (ISS) - adapted from [2] - (Permission to reuse to IEEE will be done prior publication)

The whole set of possible uncertainties makes the analysis of the s-parameter measurement extremely difficult and a methodology to verify the measurement is of utmost importance. In the case of passive element characterization, the EM simulation is a very reliable tool to verify the accuracy of the measurement [5], [7]. But in the case of active devices this approach is not applicable and alternative routes must be explored. First, one can compare compact model simulation results to calibrated and de-embedded measurements but this method does not bring insight by itself since high frequency parameters are not calibrated at the first stage of the study. Indeed, the compact model requires parameter tuning or extraction for lateral and vertical non-quasi-static effects as well as for substrate model but this cannot be performed without considering the influence of the measurement environment and of the calibration-de-embedding procedure at such high frequency. Another procedure is a direct comparison between the calibrated and de-embedded measurement to TCAD data [20]. This method has the advantage of having accurate frequency-dependent s-parameters and figures of merit (FOM) allowing one to differentiate the physical effects from any unwanted or unexpected effects coming from the measurement set-up and procedure. Unfortunately, setting up a TCAD approach is a very complex task and is not considered in this work.

In this work for the first time a new multi-physics approach combining electromagnetic simulation with SPICE simulation is proposed to emulate the complete active device embedded in

the measurement environment including probes, pads and test structures. This approach helps to clearly distinguish the transistor behavior from measurement set-up contribution. Also, the HICUM parameters correlated to high frequency, i. e., lateral, vertical non-quasi-static effects (NQS) and substrate part are tuned by integrating the EM environment, calibration and de-embedding.

The first part of the paper presents the calibrated compact model validated in the lower frequency band. In the second part, the test structures as well as the EM simulation and EM-SPICE co-simulation procedure are presented. The third part presents the results, concludes on the multi-physics approach and discusses the accuracy of the HBT measurement. The optimization of the on wafer TRL calibration and de-embedding procedure is finally proposed.

II. CALIBRATION OF THE COMPACT MODEL

The first step consists in parameter extraction for the electrical compact model. For this purpose, DC and s-parameter measurements up to 40GHz on specific test structures are required. The B55 technology [16] from STMicroelectronics was used with the standard HBT having an emitter area of $0.09 \times 4.8 \mu m^2$ and the HICUM model [17], [18], [22] has been selected for its accuracy. The s-parameter measurements are performed using a SOLT calibration on CSR8 calibration substrate and |Z|-probe. To assess the accuracy of the compact model and the associated model parameter set, the Gummel plot, output curves, transit frequency f_T and maximum oscillation frequency f_{MAX} curves are shown in Figs. 2 (a), (b), (c), and (d) respectively.
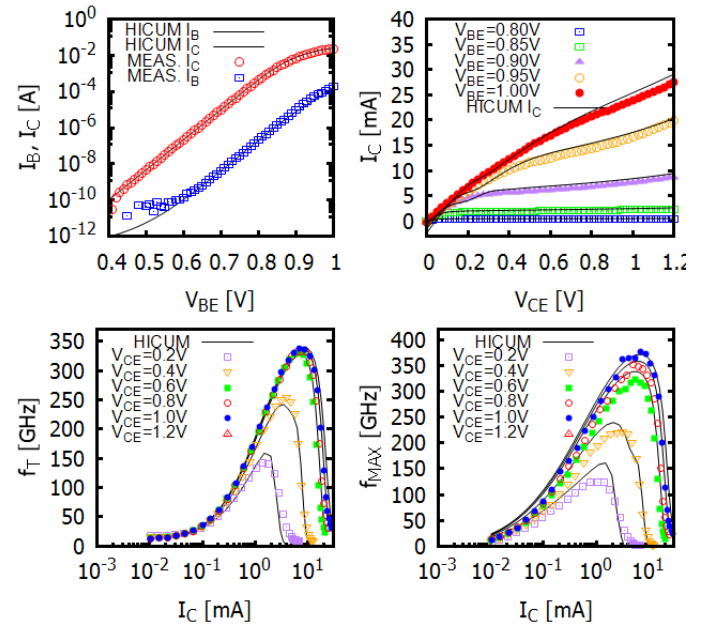

Fig. 2: Verification of HICUM model simulation with measurement: a) Gummel plot, b) Output curves, c) Transit frequency, d) Maximum oscillation frequency- B55 technology HBT 0.09*4.8µm² from STMicroelectronics-c and d are computed at 38 GHz.

III.   EM AND EM-SPICE SIMULATION

A.   Test structures

The layout of the test structures is presented in Fig. 3. It is an optimized version of the test structures compared to [19]: it is dedicated to on-wafer TRL calibration with a large space between structures and it uses staggered test structures to reduce the influence of adjacent structures. Also, the pad geometry has been optimized to be compatible with 100 and 50 µm pitch for millimeter-wave and sub-millimeter-wave measurements.
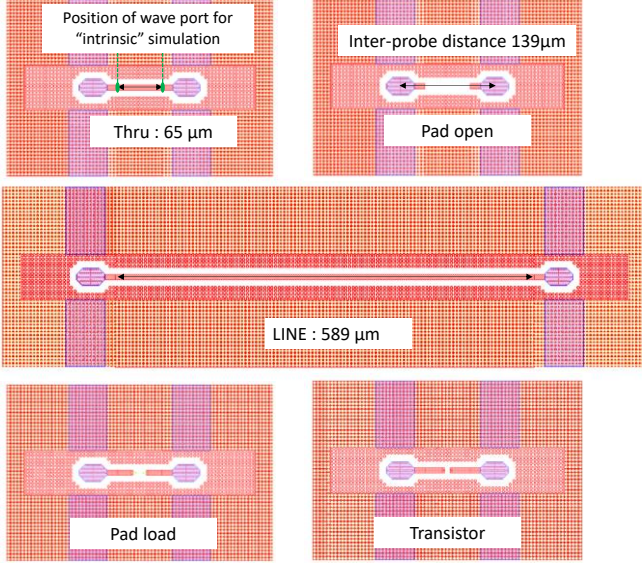

Position of wave port for "intrinsic" simulation

Thru : 65 µm

Inter-probe distance 139µm

Pad open

LINE : 589 µm

Pad load

Transistor

Fig. 3: Layout of the main test-structures used for TRL calibration and de-embedding - B55 technology- STMicroelectronics

B.   EM simulation

As described in [3], [13], [14], and in order to mimic the measurement environment, the probes are simulated together with the pads, access lines and intrinsic structures. Also, realistic probe models have been elaborated for each frequency band as shown in Fig. 4. The simulation is performed for thru (95µm including access line), reflect, line 1 (215 µm, not shown on Fig. 3), line 2 (619µm), load, transistor-open, transistor-short and finally a specific structure for the transistor that will be described in part C. The set of lines allows an accurate calibration from about 15 GHz to 500 GHz. EM simulation has shown that higher order propagation modes are canceled thanks to the scaling of the microstrip line.
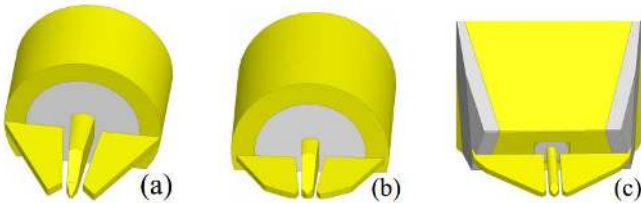

Fig. 4. EM probe models corresponding to (a) 1 GHz -110 GHz, (b) WR5, (c) WR3.4 and WR2.2. In all models, white=coaxial insulator, gray=solder, yellow=metal.

Also this is confirmed by the fact that the permittivity is constant within the frequency band starting from 20 GHz (see Fig. 5). The whole set of simulation data is computed using

exactly the same procedure as done in the measurement applying a TRL calibration followed by the short-open de-embedding. We call it "EM simulated experimental procedure" or EM SimExP.
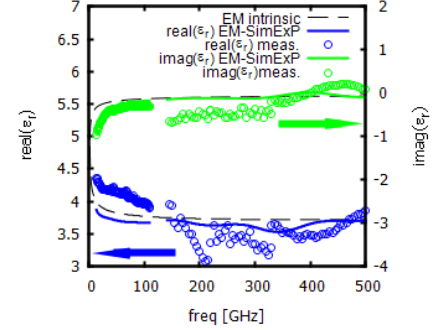

Fig. 5. a) Real and imaginary part of the effective dielectric, measurement, EM and EM intrinsic simulation. (Intrinsic simulation means that the EM port have been considered after the pad, see fig. 3)

C.   EM-SPICE co-simulation

The next step consists in adding the intrinsic transistor (represented by the compact model simulation results) to the EM simulation environment. In order to have simulation data of the transistor embedded with vias, access lines, pads and probes, we modify the EM transistor-open structure adding two lumped ports for base and collector to connect the EM structure to the SPICE model. Hence, using an s-parameter box, we associate the 4 port matrix of the EM simulation (2 ports at the probe, one port for the base and one port for the collector) to the two-port matrix of the HBT. The whole procedure is described in Fig. 6(b) and the EM simulation structure is described in Fig. 6(a). In that case, we call it "EM-SPICE simulated experimental procedure" or EM-SPICE SimExP.

IV.   MEASUREMENT METHODOLOGY

Four measurement benches were used to cover the frequency range from 1 GHz to 500 GHz. First, we choose a E8361A Vector Network Analyzer (VNA) from Agilent working up to 110 GHz and using extenders (N5260-60003) above 67 GHz. Then, for the different frequency bands 140-220 GHz, 220-330 GHz and 325-500 GHz, measurements were carried out with a four port Rohde & Schwarz ZVA24 VNA, coupled with Rohde & Schwarz VNA extenders (ZC220-ZC330-ZC500). The extenders are installed on a PM8 Cascade probe station. The power level is approximately set to less than -32 dBm at the output of mmW head in the four bands for the measurement of active and passive elements. The probes used in this work are Picoprobe with a 50 µm pitch (GGB industries) in each frequency band except below 110 GHz where the probes have a 100 µm pitch.

Transistor EM sim. with 4 ports

P2

P1

a) 4 ports EM simulation structure, zoom of bottom view of half structure

Ci, P4

Bi, P3

Ci

Bi

SPICE - HICUM 2 port

EM simulation 4 port

Transistor EM–SPICE 2 port

TRL calibration procedure

De-embedding

Thru, Reflect, Lines, Load, Trans.-open, Trans.-short
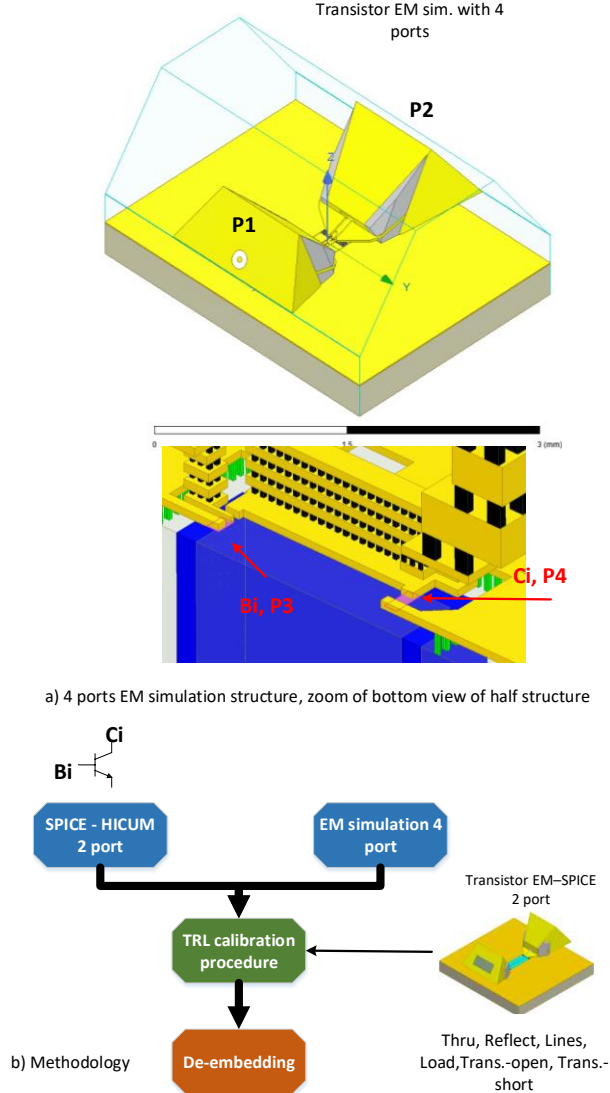
b) Methodology

Fig. 6: a) EM simulation structure with zoom on bottom view for the transistor simulation, b) Description of the EM-SPICE simulation of experimental procedure (SimExP) used to simulate the transistor calibration with de-embedding including the EM environment.

Moreover, raw on-wafer measurements data have been recorded only to be post-processed by our in-house calibration tool to perform on-wafer TRL calibration.

V. RESULTS

A. Analysis

In a first step, the consistency of the EM probe models was investigated by comparing the measurement and simulation of the passive elements structures. Figs. 7(a) and 7(b) present the calibrated transistor-open and transistor-short data up to 500 GHz, respectively.

The trends of the capacitor and inductor values are well described and clearly highlight the quality and accuracy of the EM models. Below 110 GHz, the measurement is noisier due to the fact that VNA equipment is from an older generation; nevertheless we can identify the unexpected behavior above 70 GHz with a drop of the C_{12} capacitance value. In WR5 band, the C_{12} capacitance becomes negative; this can be attributed to

a pronounced probe-to-substrate coupling as well as the probe-to-probe coupling in this band. The probe design and the pad layout are visibly incompatible in this frequency band. In addition, inaccuracies in the probe-pad contact were observed in this WR5.1 band, which increases the difficulty of comparing simulation and experiment. In contrast, the calibration in WR3.4 and 2.2 band gives more realistic results. As shown in [19], this is attributed to highly downscaled probes restraining and guiding the EM field towards the structure in a confined way.
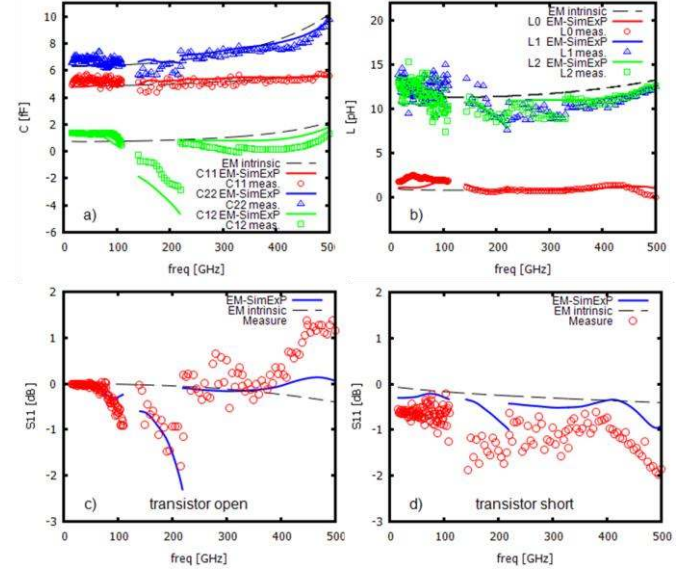

Fig. 7: a) Capacitances of the transistor-open; b) Inductors of the transistor-short; c) S11 of transistor open, d) S11 of transistor short; measurement (symbols), EM SimExP (EM with probe and calibration) (solid line) and EM intrinsic simulation (dashed line) up to 500 GHz using an on-wafer TRL (thru of 65µm) - B55 technology - STMicroelectronics

In a second step, the EM-SPICE co-simulation is carried out. The s-parameters of the probes with the pads and access lines and the compact model are concatenated. Then, these new s-parameters are calibrated using the error terms obtained by the TRL calibration and finally a short-open de-embedding is performed. Assuming a perfect calibration method and a full valid de-embedding procedure, the obtained results are expected to match perfectly with the compact model simulation results. Thus, we obtain and compare three different data sets: (i) the calibrated/de-embedded measured data, (ii) the EM-SPICE (calibrated/de-embedded data from EM-SPICE co-simulation) and (iii) the compact model data.

First, we consider the comparison of the data sets (i) and (ii) that is to say, measurement and EM-SPICE SimExP data. This comparison helps us to understand if some unexpected trends in the measured results are intrinsically correlated to the measurement setup or are due to a user error: The error can be the probe positioning, the probe contact difficulties, the probe tilt or any inaccuracy within the probe's installation. The user error can be completely avoided in EM-SPICE co-simulation data. Fig. 8 presents magnitude and phase of the s-parameters for two different operating points up to 500 GHz. Analyzing the phase of S_{11}, we observe that after a typical monotonous decrease of the phase up to about 250-330 GHz (bias point dependent), a slight increase of the phase appears and then

again decreases after 450 GHz. While these effects, in general, are termed as unexpected and questionable, the co-EM-SPICE simulation reproduces the same. Since the eventual measurement uncertainties are suppressed in EM-Spice co-simulation, we deduce that the measurements are correct and the observed phenomenon is correlated to the methodology, to the probes and/or to the design of the test structures.
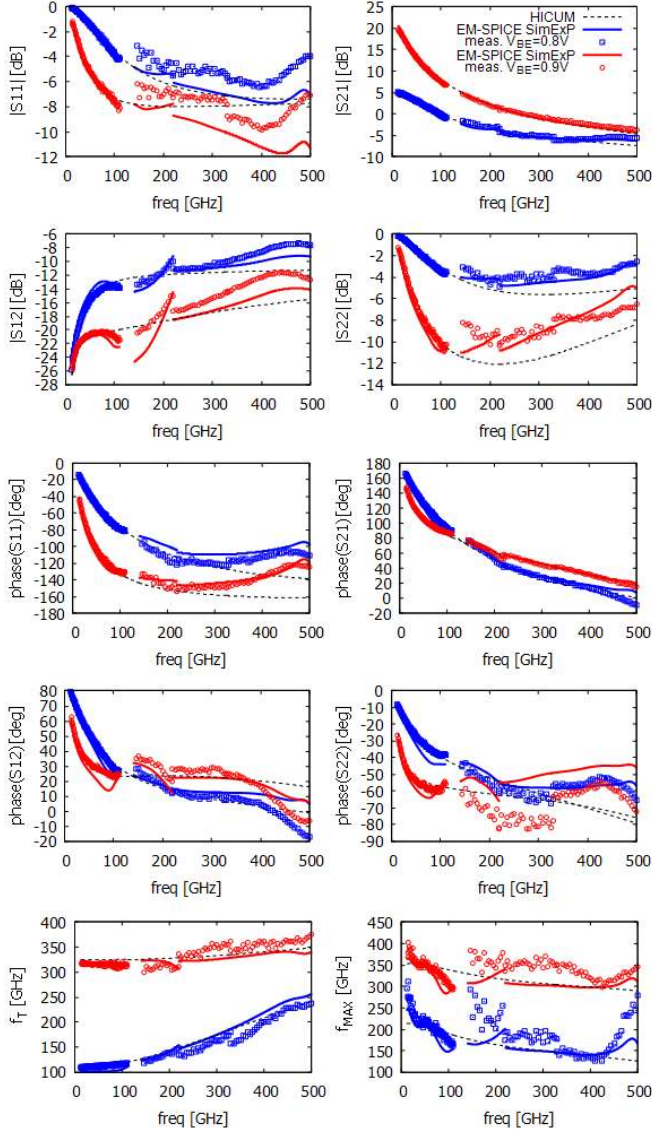

Fig. 8: Magnitude and phase of the S parameters for two different operating points, transit frequency and maximum oscillation frequency extrapolation. Measurement (symbols), EM-SPICE SimExP data (EM-HICUM with probe with calibration-de-embedding) (solid line) and HICUM simulation (dashed line). Both are calibrated using an on-wafer TRL (reference plane: through of 65µm) with de-embedding - Dashed line is HICUM model of the transistor (B55 technology- STMicroelectronics).

Second, we compare the calibrated and de-embedded EM-SPICE co-simulation results of the transistor to the compact model data and use the former data as a reference. As already said, if the calibration/de-embedding methodology is faultless, the calibrated data will perfectly match the compact model data. In case of a divergence, we can conclude that the calibration method or the de-embedding procedure has some limitations in term of accuracy or their applicability is questionable in certain frequency bands. Keeping the example of the phase of S_{11} and

comparing it to the reference data where a continuous decrease of the phase up to 500 GHz for both operating points can be noticed, we conclude that the calibration methodology together with the de-embedding procedure doesn't allow to obtain the expected results accurately above 250-330 GHz (bias point dependent).

Extending this approach to the whole set of s-parameters, we identify three types of mismatch that were observed in both the measurement and the EM-SPICE co-simulation with respect to the reference data. The first is related to the reflection coefficients S_{11} and S_{22}, the second to the band discontinuity between two frequency bands and the third to the transmission coefficients S_{12} and S_{21} as explained here. First, the magnitude and phase of S_{11} as well as the phase of S_{22} show an unexpected behavior above 350-400 GHz. Secondly, some discontinuities appear at the band transition at 220 GHz considering the lower band WR5.1 and the upper band WR3.4. This is observed for measurement as well as in the EM-SPICE co-simulation and can be attributed to the probe-to-substrate coupling which is strong in the case of the WR5 band, but much less pronounced in the WR3.4 band. Third, the magnitude of S_{21} shows a slight change in slope above 400 GHz at V_{BE}=0.8 V which is also observed through EM-SPICE co-simulation. This is attributed to crosstalk and confirmed also by an unreliable value of S_{12} above 400 GHz.
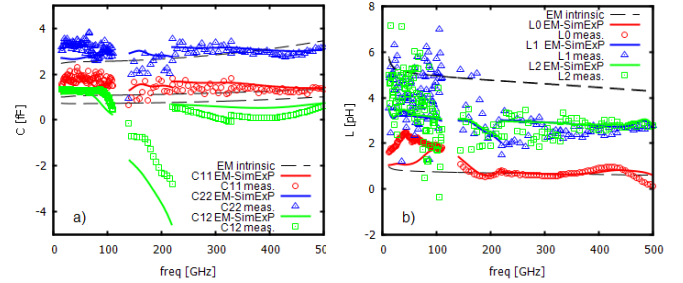

Fig. 9. a) Capacitances of the transistor open; b) Inductors of the transistor short; measurement (symbols), EM SimExP (solid line) and EM intrinsic simulation (dashed line) up to 500 GHz using an on-wafer TRL with the second reference plane (thru of 15µm) - B55 technology- STMicroelectronics

More unexpectedly (and barely visible on s-parameters in the frequency range from 50 GHz to 110 GHz), a change of the slope of mag(S_{12}) is observed which can also be attributed to the cross-talk effect. Please note that a similar effect has been observed on C_{12} (see Fig. 7a) for the transistor-open structure. Although the effect on S_{12} seems to be negligible, it has a strong impact on f_{MAX} (see Fig. 8) with an unexpected and significant reduction on f_{MAX} beyond 50 GHz that remained unexplained for a long time.

B. Improvement of the calibration/de-embedding methodology

The results presented above show that the measured data and the EM-SPICE co-simulation are reasonably well aligned, but differ from the compact simulation data over a certain frequency range, requiring us to review the calibration and de-embedding procedures. In order to improve the calibration methodology, two main routes can be explored. The first one concerns the cross-talk above 400 GHz which requires to modify the probe-to-probe distance on the test-structures but that can be only investigated in a future chip design. The second one concerns the reflection s-parameters. Observing the

transistor-open and transistor-short measurement and simulation results in Fig. 7, the capacitances and inductances are not completely constant with frequency. This frequency dependence (0.6fF / 100 GHz bandwidth) demonstrates a typical distributed behavior of the capacitance and is attributed to the access line. Hence, an easy way to proceed is to move the reference plane that is set at 15 µm after the pad to 40 µm after the pad. Doing so, by exploiting the same test structures design and raw measurements, the calibration plane is set closer to the DUT by simple matrices manipulation, so that the distributed effects are strongly reduced as observed for the capacitance and inductors (see Fig. 9).
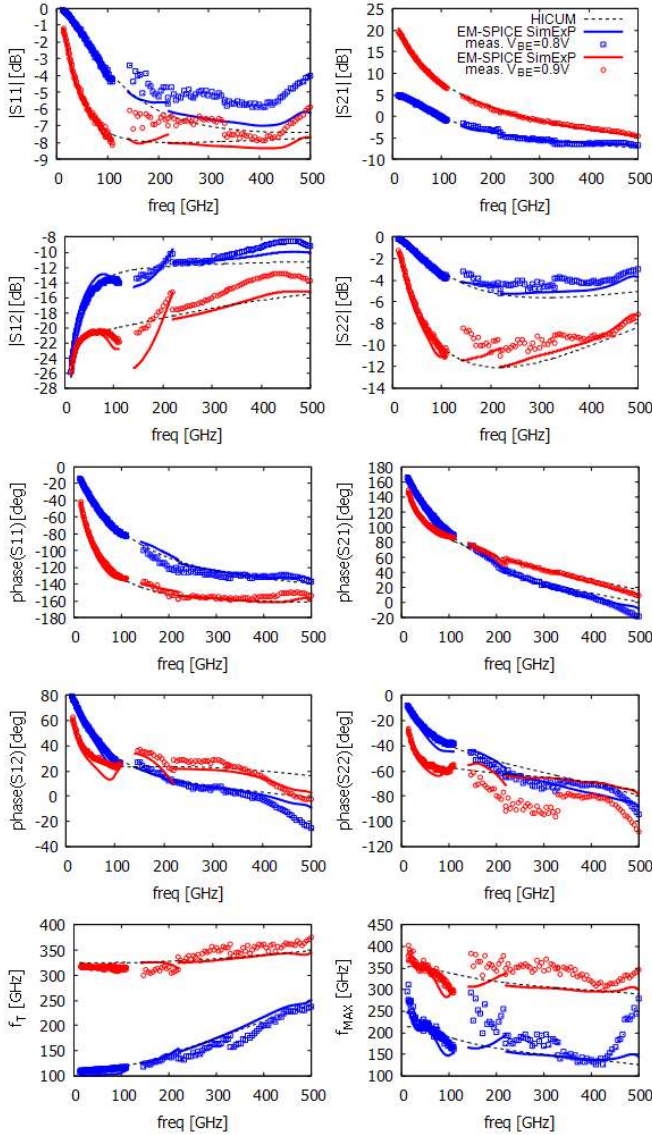

Fig. 10: Magnitude and phase of the S parameters, transit frequency and maximum oscillation frequency extrapolation. Measurement (symbols), EM-SPICE SimExP data (EM-HICUM with probe with calibration-de-embedding) (solid line) and HICUM simulation (dashed line). Both are calibrated using an on-wafer TRL (reference plane: through of 15µm) with de-embedding- Dashed line is HICUM model of the transistor (B55 technology- STMicroelectronics).

Applying this reference plane shift to the TRL then improves the accuracy of the phase of S_{11} and S_{22} in both the EM-SPICE

co-simulation and the measurement, and they are approaching the compact model data used as reference (see Fig. 10 and Fig. 11). Also, an improvement can be observed for the magnitude of S_{11} and S_{22}. On can note that the three sets of data, measurement, EM-SPICE co-simulation and reference, do not perfectly converge for the magnitude of S_{11}. This is attributed to a perfectible calibration of the lateral non-quasi static effects in the HICUM model. Finally, an improvement is also noted for the maximum oscillation frequency but only at very high frequencies above 220 GHz.

Below 220 GHz, the f_{MAX} curve is still questionable. In order to clarify the artefacts, we use the highly downscaled probe from the WR3.4 & WR2.2 band to simulate the calibration/de-embedding procedure also for the lower frequency bands since this downscaled probe is less prone to cross-talk. Doing so and analyzing the magnitude of S_{12}, we can observe that the unexpected decrease of S_{12} above 50 GHz is suppressed. Fig 11 shows the difference between the EM-SPICE SimExP data to the reference (HICUM model). The figure indicates that the error on magnitude of S_{12} with the set of probes used in experiment rises to 3 dB at 110 GHz and up to 6 dB at 220 GHz while with the WR3.4 & WR2.2 probe the difference is limited to less than 1 dB over the whole frequency band.

Moreover, the surprising frequency behavior observed for WR5 (140-220 GHz) band with strong discontinuities at the band edge is also suppressed. This can be explained by a decreased probe-to-substrate coupling as well as a reduced crosstalk thanks to a better design of the probe that helps to confine the EM field [19]. Secondly, this modification noticed for S_{12} directly affects the f_{MAX} value. The previously observed sudden decrease for f_{MAX} at a frequency higher than 50 GHz is quasi suppressed when using an optimized probe geometry. For example, the error for f_{MAX} measurement is reduced by a factor four at 110GHz. The same observation can be made in the WR5 band (140-220 GHz) where the unexpected monotonic increase of f_{MAX} is replaced by a monotonic decrease. Hence, the commonly known noisy f_{MAX} curve is strongly impacted by the measurement set-up, especially by the probes topology, the layout of the pads and test structures. Therefore, the double verification of f_{MAX} with two different benches having different probes as demonstrated in [3] and shown in Fig. 1 is very relevant. In summary, the change in the TRL reference plane closer to the DUT and the use of optimized probe such as the WR2.2 from Picoprobe GGB shows that the measurement can be performed with an accuracy better than 0.3 dB in terms of magnitude and 5 degree in terms of phase of S parameters for this particular test structures up to 400 GHz. f_T and f_{MAX} measurement accuracy would be better than 5% which is very reasonable.
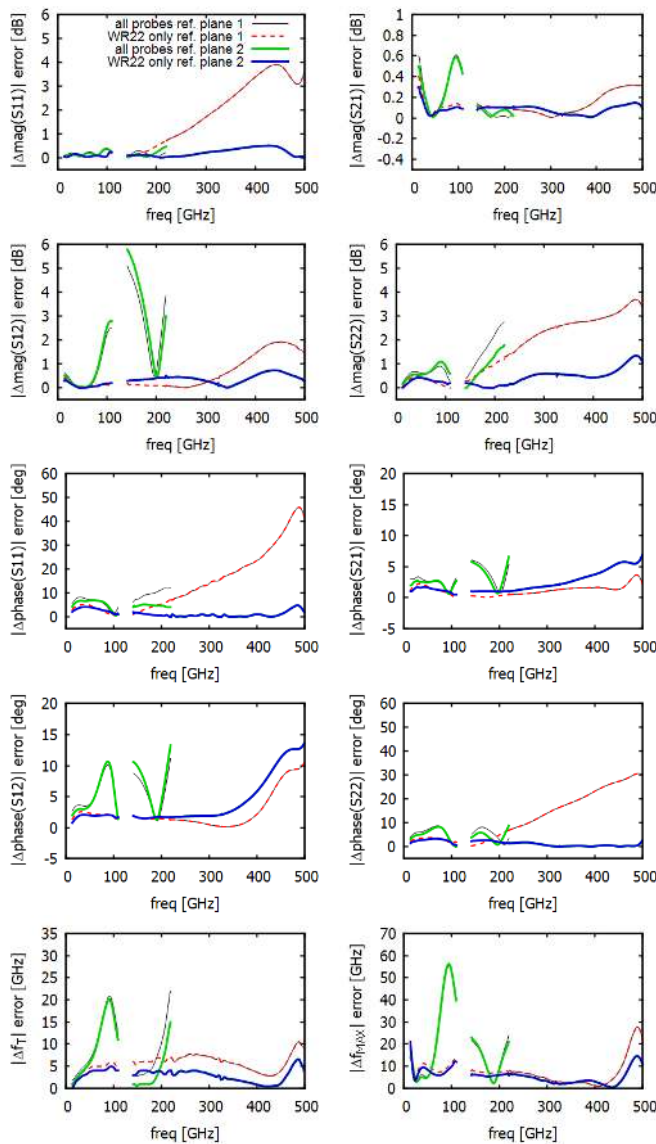
Fig. 11. Error assessment for EM-SPICE SimExP data using a WR2.2 (325-500 GHz) for the whole frequency band (1-500GHz) compared to the EM-SPICE SimExP using each probe topology of fig. 4 and for the two calibration reference plane (14.5 and 65 µm): Magnitude and phase of S parameter, error in GHz for the transit frequency and maximum oscillation frequency extrapolation..

VI. CONCLUSION

A simulation methodology using EM-SPICE approach is proposed to verify the consistency of high frequency transistor measurements. This new method is based on EM-SPICE co-simulation including the simulation of the RF probes, the pads, the access lines as well as all the DUTs and to apply the on-wafer TRL calibration and de-embedding procedure. Although, this method is applied to SiGe HBT in this work, it can be directly transferred to III-V HBTs, HEMTs, or silicon FET transistors which face similar issues in high frequency measurements.

With this method we have clearly identified some artefacts that can be attributed to a combination of different effects such as probe-to-substrate coupling, calibration together with de-embedding method and layout design. The unexpected trend of the key figures of merit i. e. the f_{MAX} of high speed transistors

has been explained for the first time. One possible solution of the f_{MAX} measurement improvement requires the downscaling of probes below 220 GHz.

VII. REFERENCES

[1] P. Hillger, J. Grzyb, R. Jain, et U. R. Pfeiffer, « Terahertz Imaging and Sensing Applications With Silicon-Based Technologies », *IEEE Trans. Terahertz Sci. Technol.*, vol. 9, nº 1, p. 1-19, janv. 2019, doi: 10.1109/TTHZ.2018.2884852.

[2] V. Teppati, S. Tirelli, R. Lövblom, R. Flückiger, M. Alexandrova, et C. R. Bolognesi, « Accuracy of Microwave Transistor $_{\rm T}$ and $_{\rm MAX}$ Extractions », *IEEE Trans. Electron Devices*, vol. 61, nº 4, p. 984-990, avr. 2014, doi: 10.1109/TED.2014.2306573.

[3] B. Heinemann *et al.*, « SiGe HBT with fx/fmax of 505 GHz/720 GHz », in *2016 IEEE International Electron Devices Meeting (IEDM)*, déc. 2016, p. 3.1.1-3.1.4, doi: 10.1109/IEDM.2016.7838335.

[4] C. B. Sia, « Minimizing discontinuities in wafer-level sub-THz measurements up to 750 GHz for device modelling applications », in *2017 89th ARFTG Microwave Measurement Conference (ARFTG)*, juin 2017, p. 1-4, doi: 10.1109/ARFTG.2017.8000843.

[5] S. Fregonese *et al.*, « On-Wafer Characterization of Silicon Transistors Up To 500 GHz and Analysis of Measurement Discontinuities Between the Frequency Bands », *IEEE Trans. Microw. Theory Tech.*, p. 1-10, 2018, doi: 10.1109/TMTT.2018.2832067.

[6] K. Yau, E. Dacquay, I. Sarkas, et S. P. Voinigescu, « Device and IC Characterization Above 100 GHz », *IEEE Microw. Mag.*, vol. 13, nº 1, p. 30-54, janv. 2012, doi: 10.1109/MMM.2011.2173869.

[7] S. Fregonese *et al.*, « Comparison of On-Wafer TRL Calibration to ISS SOLT Calibration With Open-Short De-Embedding up to 500 GHz », *IEEE Trans. Terahertz Sci. Technol.*, vol. 9, nº 1, p. 89-97, janv. 2019, doi: 10.1109/TTHZ.2018.2884612.

[8] R. Sakamaki et M. Horibe, « Uncertainty Analysis Method Including Influence of Probe Alignment on On-Wafer Calibration Process », *IEEE Trans. Instrum. Meas.*, vol. 68, nº 6, p. 1748-1755, juin 2019, doi: 10.1109/TIM.2019.2907733.

[9] G. N. Phung *et al.*, « Influence of Microwave Probes on Calibrated On-Wafer Measurements », *IEEE Trans. Microw. Theory Tech.*, vol. 67, nº 5, p. 1892-1900, mai 2019, doi: 10.1109/TMTT.2019.2903400.

[10] M. Seelmann-Eggebert *et al.*, « On the Accurate Measurement and Calibration of S-Parameters for Millimeter Wavelengths and Beyond », *IEEE Trans. Microw. Theory Tech.*, vol. 63, nº 7, p. 2335-2342, juill. 2015, doi: 10.1109/TMTT.2015.2436919.

[11] C. Andrei, D. Gloria, F. Danneville, P. Scheer, et G. Dambrine, « Coupling on-wafer measurement errors and their impact on calibration and de-embedding up to 110 GHz for CMOS millimeter wave characterizations », in *2007 IEEE International Conference on Microelectronic Test Structures*, mars 2007, p. 253-256, doi: 10.1109/ICMTS.2007.374494.

[12] G. N. Phung, F. J. Schmückle, et W. Heinrich, « Parasitic effects and measurement uncertainties in multi-layer thin-film structures », in *2013 European Microwave Conference*, oct. 2013, p. 318-321, doi: 10.23919/EuMC.2013.6686655.

[13] F. J. Schmückle, T. Probst, U. Arz, G. N. Phung, R. Doerner, et W. Heinrich, « Mutual interference in calibration line configurations », in *2017 89th ARFTG Microwave Measurement Conference (ARFTG)*, juin 2017, p. 1-4, doi: 10.1109/ARFTG.2017.8000823.

[14] W. Quan, A. M. Arabhavi, R. Flueckiger, O. Ostinelli, et C. R. Bolognesi, « Iterative De-Embedding and Extracted Maximum Oscillation Frequency f_MAX in mm-Wave InP DHBTs: Impact of Device Dimensions on Extraction Errors », in *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, oct. 2018, p. 110-113, doi: 10.1109/BCICTS.2018.8550904.

[15] A. M. Mangan, S. P. Voinigescu, M.-T. Yang, et M. Tazlauanu, « De-embedding transmission line measurements for accurate modeling of IC designs », *IEEE Trans. Electron Devices*, vol. 53, nº 2, p. 235-241, févr. 2006, doi: 10.1109/TED.2005.861726.

[16] P. Chevalier *et al.*, « A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz fT / 370 GHz fMAX HBT and high-Q millimeter-wave passives », in *2014 IEEE International Electron Devices Meeting*, déc. 2014, p. 3.9.1-3.9.3, doi: 10.1109/IEDM.2014.7046978.

[17] M. Schroter, M. Friedrich, et H.-M. Rein, « A generalized integral charge-control relation and its application to compact models for silicon-based HBT's », *IEEE Trans. Electron Devices*, vol. 40, nº 11, p. 2036-2046, nov. 1993, doi: 10.1109/16.239746.

[18] M. Schroter et Tzung-Yin Lee, « Physics-based minority charge and transit time modeling for bipolar transistors », *IEEE Trans. Electron Devices*, vol. 46, nº 2, p. 288-300, févr. 1999, doi: 10.1109/16.740893.

[19] C. Yadav, « Importance and Requirement of frequency band specific RF probes EM Models in sub-THz and THz Measurements up to 500 GHz », IEEE Trans. Terahertz Sci. Technol., DOI: 10.1109/TTHZ.2020.3004517

[20] Soumya Ranjan Panda, Sebastien Fregonese, Anjan Chakravorty, Thomas Zimmer, "TCAD simulation and assessment of anomalous deflection in measured S-parameters of SiGe HBTs in THz range", IEEE BCICTS, Nashville, USA, 2019, DOI: 10.1109/BCICTS45179.2019.8972760

[21] Uwe Rüddenklau, Michael Geen, Andrea Pallotta, Mark Barrett, Piet Wambacq, Malcolm Sellars, https://www.etsi.org/images/files/ETSIWhitePapers/etsi_wp15_m wt_semiconductor_technology.pdf, p9, 2016.

[22] M. Schroter and A. Pawlak, https://www.iee.et.tu-dresden.de/iee/eb/forsch/Hicum_PD/Hicum23/hicum_L2V2p4p0_ manual.pdf