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A new family of soft transition converters: Design and dynamic model

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Abstract. The soft switching converters evolved through the resonant load, resonant switch, resonant transition and active clamp converters to eliminate switching losses in power converters. This paper briefly presents the operating principle of the new family of soft transition converters; the methodology of design of these converters is presented through an example. In the proposed family of converters, the switching transitions of both the main switch and auxiliary switch are lossless. When these converters are analysed in terms of the pole current and throw voltage, the defining equations of all converters belonging to this family become identical. Such a description allows one to define simple circuit oriented model for these converters. These circuit models help in evaluating the steady state and dynamic model of these converters. The standard dynamic performance functions of the converters are readily obtainable from this model. This paper presents these dynamic models and verifies the same through measurements on a prototype converter.

Keywords. Resonant converters; ZVS; ZCS; Auxiliary switch converters; Coupled inductor.

1. Introduction

The constant demand for smaller and lighter power DC–DC converters is pushing the switching frequencies well into Mega Hertz range. Such high frequency switching is possible by resonant topologies (Vatche Vorperian 1984; Zheng *et al* 1986; Claudio Manoel *et al* 1995; Hua *et al* 1994; Moschopoulos *et al* 1995; Moschopoulos *et al* 1999; Yingqi Zhang *et al* 2001; Moschopoulos & Jain 2003; Youhao Xi & Jain 2003; Moschopoulos & Jain 2004; Wang 2006; Smith & Smeley 1994; Freitas & Gomes 1993; Laksminarasamma *et al* 2004).

Quasi-resonant converters (QRC) introduced in Zheng *et al* (1986) reduce the switching losses in PWM converters operating at high switching frequency. The control for this family of converters is by variable switching frequency. However, the switches in QRC are subjected to high voltage stress and/or high current stress (Freeland & Middlebrook 1987).

In zero-voltage transition (ZVT) converters, introduced in Hua *et al* (1994), the VA ratings of the switches are same as that of the source voltage and load current. However, the auxiliary switches still have switching losses during turn-off.

Several zero voltage transition (ZVT) topologies have been proposed (Hua *et al* 1994; Wang 2006). All these topologies have an auxiliary circuit, added to the pwm counter part. This ensures soft turn-off of the passive switch and ZVS turn-on of the active switch. The ZVT converters proposed in literature have the following features.

(i) Turn-off of the auxiliary switch is lossy
(ii) The auxiliary switch requires a floating gate drive
(iii) The additional components count is more
(iv) VA rating of the switch is higher than the source voltage and the load current
(v) The lossless switching is load-dependent.

A new family of soft transition converters was proposed in 2007 (Lakshminarasamma & Ramanarayanan 2006; 2007). The proposed scheme (Lakshminarasamma & Ramanarayanan 2006; 2007) employs an auxiliary circuit. The auxiliary circuit consists of a dependent source, auxiliary switch, auxiliary diode and a pair of resonant elements. Soft turn-on transitions of the main and the auxiliary switch are obtained by the resonant elements. Soft turn-off of the auxiliary switch is enabled by the dependent source. The soft turn-off transition of the main switch is assisted by the resonant capacitor. The switching transitions of both the main switch and auxiliary switch are lossless. The switching frequency is constant. The VA ratings of the active switch are same as that of the throw voltage and pole current. The VA ratings of the auxiliary switch are more than the throw voltage and the pole current; however conduction period of the auxiliary switch is only from 15% to 20% of the switching period. The proposed circuit can be applied to most of the isolated and non-isolated DC–DC converters.

The proposed scheme introduces an auxiliary circuit parallel to the main switch. The auxiliary circuit is shown in figure 1. The auxiliary circuit consists of a dependent source V_a, auxiliary switch S_a, auxiliary diode D_a and a pair of resonant elements L_a and C_a. The dependent source V_a serves the purpose of achieving lossless reset of the auxiliary circuit. The novelty in the proposed circuit is the method of generating the dependent voltage required to ensure ZCS of the auxiliary switch. The dependent source is realized by a coupled winding in the energy storage inductor of the DC–DC converter.

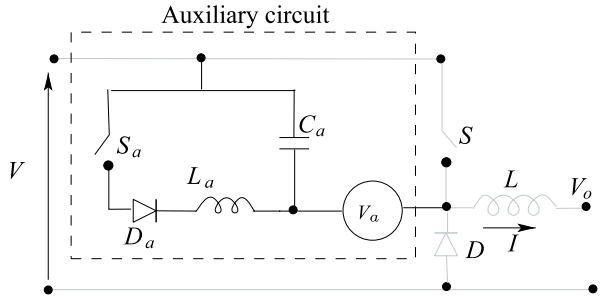


Figure 1. Auxiliary circuit cell.

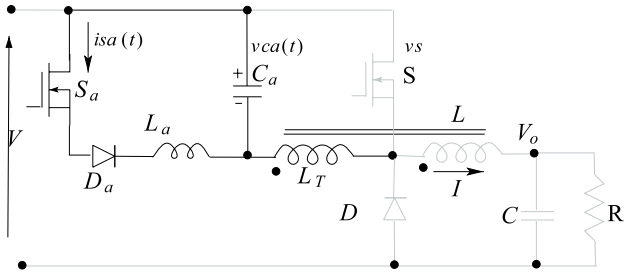


Figure 2. Buck converter with primitive auxiliary switch commutation circuit.

The auxiliary circuit when switched properly, ensures lossless switching. This paper briefly presents the operating principle of this family of converters; the methodology of design of these converters is presented through an example.

This family of converters when analysed in terms of the pole current and throw voltage, the defining equations of all converters belonging to this family become identical. Such a description allows one to define simple circuit oriented model for these converters. These circuit models help in evaluating the steady state and dynamic model of these converters. The standard dynamic performance functions of the converters are readily obtainable from this model. This paper presents these dynamic models and verifies the same through measurements on a prototype converter.

The paper is organized as follows: Section 2 presents briefly the steady-state analysis of the performance of the auxiliary switch resonant transition buck converter (Lakshminarasamma & Ramanarayanan 2006; 2007). Design guidelines with a design example is presented in § 3. Unified analysis of converters are presented in § 4. The steady state and small signal equivalent circuit model of the converter topologies in the proposed circuit are presented in § 5. Sections 6, 7 and 8 present design validation and the experimental results of steady state and dynamic model of the 33 Watt, 400 KHz boost converter. Conclusion is presented in § 9.

2. Steady-state analysis of buck converter in the proposed topology

Figure 2 shows the auxiliary switch resonant transition buck converter. The commutation process and the steady-state performance is briefly explained in this section (Lakshminarasamma & Ramanarayanan 2006; 2007). The turns ratio between L and L_T may be chosen conveniently. The winding L_T has to carry the commutation current and reset current only. Therefore the RMS value of this coupled winding current will be a small fraction of the current flowing in the main inductor L. Accordingly, this will not demand a higher size of inductor. To simplify the analysis, turns ratio for the coupled inductor (L and L_T) is taken to be 1. Switching sequences are as shown in figure 2.

Prior to time $t = t_o$, the main switch S and the auxiliary switch S_a is in OFF state. The load current is freewheeling through the diode D. The resonant capacitor is charged to voltage $(V + V_0)$. The auxiliary switch S_a is turned-on with ZCS at $t = t_o$ with zero initial current in the resonant inductor L_a. The load current is freewheeling through the passive switch D. The current in the auxiliary switch will increase linearly as shown in figure 3.

The turn-off of the passive switch D is followed by the resonant interval (L_a and C_a). The auxiliary switch current $i_{Sa}(t)$ rises sinusoidally. This interval ends, when the voltage across the resonant capacitor $v_{Ca}(t)$ reaches $(V_o - V)$. This forward biases the body diode of the main switch S.

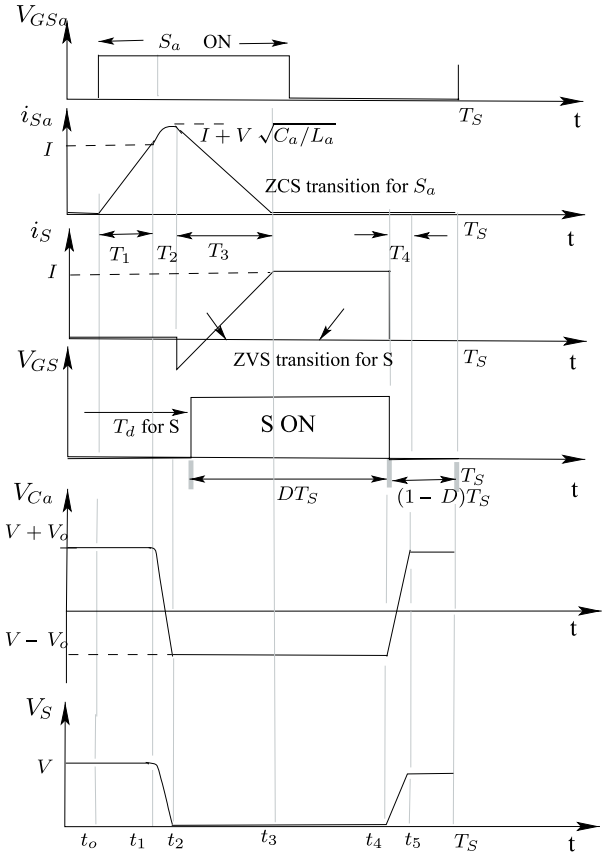


Figure 3. Switching transitions of the buck converter with auxiliary circuit.

The resonant inductor current flows through the body diode of the main switch S, auxiliary switch S_a and the auxiliary diode D_a. The turn-on of the main switch S at $t = t_2$ is zero voltage switching. The trapped energy in the auxiliary circuit inductor L_a is recovered into the coupled inductor L_T. The voltage across the resonant inductor is -$(V - V_o)$. The negative voltage across the resonant inductor L_a will reset $i_{sa}(t)$ linearly to zero at $t = t_3$ (Load current is carried by the main switch S). Turn-off of the auxiliary switch at $t = t_3$, ensures zero current switching. The main switch S turn-off is at or near zero on account of capacitor across the main switch.

3. Design guidelines

In this section, the methodology of design of auxiliary switch resonant transition converters is presented through an example. Consider a boost converter shown in figure 4.

3.1 *Selection of boost converter components*

The process of selecting boost inductor L, main switch S, main diode D, output capacitor C_o is the same as that for a conventional PWM boost converter. The design and ratings of these components are same as that of the hard switched boost converter.

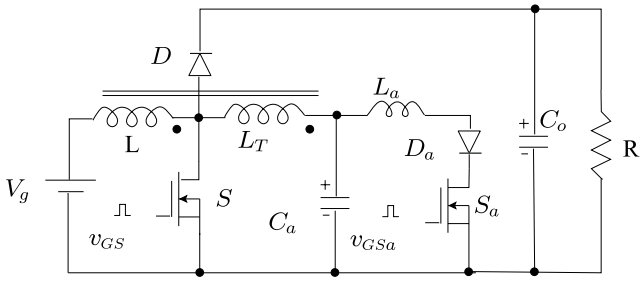


Figure 4. ZVS boost converter with auxiliary circuit.

3.2 *Selection of resonant inductor L_a and resonant capacitor C_a*

The rate of rise of current in the auxiliary circuit in the interval T_1 depends on L_a. Larger value of L_a increases the length of the resonant interval T_2. This inturn increases auxiliary circuit RMS current leading to increase in the conduction losses. The value of L_a and C_a together decides the resonant interval T_2. The resonant interval should be as minimum as possible. This reduces the conduction losses in the auxiliary switch; the effective duty cycle increases. The length of the resonant interval is approximately a quarter of the resonant period $\frac{\pi}{2}\sqrt{L_a C_a}$. The selection of the values of L_a and C_a is based on eq. 1.

$$\frac{\pi}{2}\sqrt{L_a C_a} = (5 \text{ to } 10)\% \text{ of } T_{on}(\max). \tag{1}$$

Larger values of C_a increases the auxiliary circuit current. Lower values of C_a increases rate of rise of voltage across main switch. Value of C_a is selected such that the voltage across the main switch does not exceed the specified limit. The selection of C_a is based on eq. 2.

$$C_a = \frac{I\, t_f}{2\, V}. \tag{2}$$

I is the on-state current, V is the off-state voltage, t_f is the fall time of the main switch.

3.3 *Selection of auxiliary switch S_a, auxiliary diode D_a and freewheeling diode D*

The device used for the auxiliary switch should be with a lower output capacitance. This minimizes the turn-on losses due to discharge of the junction capacitance of the switch. Fast recovery diodes are used for auxiliary diode D_a and freewheeling diode D.

3.3a *Gate signals of the auxiliary switch S_a and the main switch S:* The gate signals to S and S_a are as shown in figure 5 to ensure ZVS and ZCS transitions of the main and the auxiliary switch respectively. The turn-on of auxiliary switch is at zero current. The minimum on time of the auxiliary switch is $t = T_1 + T_2 + T_3$. This ensures that the turn-off transition of the auxiliary switch S_a is at zero current. The minimum delay T_d for the turn-on of the main switch S is $t = T_1 + T_2$. In the proposed circuit, since the capacitors are ground referenced or power supply referenced, it is possible to programme the delay between the auxiliary switch and the main switch dependent on the capacitor voltage to sense the completion of the resonant process. The control scheme shown in figure 6 may be used to overcome this problem. This serves the dual purpose of reducing the switching loss close to zero and not getting the body diode of the main switch to conduct.

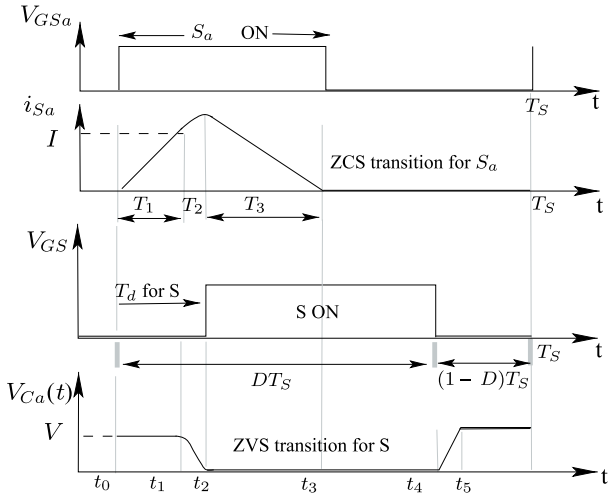


Figure 5. Gate signals of the auxiliary switch and the main switch S.

Based on the above design guidelines, a design procedure to select the components of the proposed circuit for boost topology is presented in this paper.

4. Unified analysis of converters

Unified steady state analysis for the new family of converters is presented in terms of pole current and throw voltage. These converters have three sub-intervals per cycle. Further, the circuit equations governing these sub-intervals are identical when expressed in terms of pole current and throw voltage (I, V). It is seen that the steady state and dynamic equivalent circuits can be obtained from this idealized analysis. Analytical expressions for DC conversion ratio of all topologies may be derived in terms of pole current and throw voltage (discussed in the next section).

The pole current and the throw voltage for non-isolated converters are defined as shown in table 1. With the definitions given in table 1, the circuit equations governing the sub-intervals are identical and are shown in table 2. The resonant capacitor voltage $v_{Ca}(t)$ and the resonant inductor current $i_{La}(t)$ equations in the three main sub-intervals are shown in table 2.

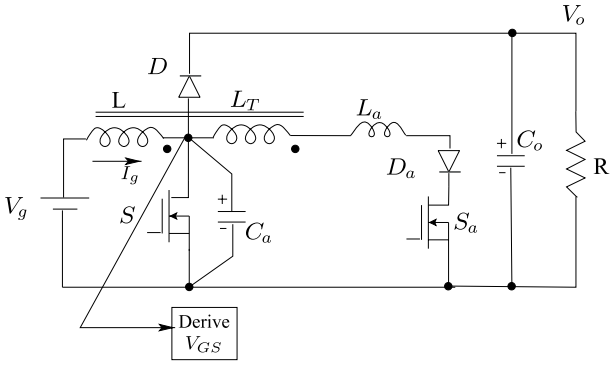


Figure 6. Derivation of the switch delay based on the capacitor voltage.

Table 1. Definition of pole current and throw voltage for non-isolated converters.

Converter	Throw voltage V	Pole current I
Buck	V_g	I_o
Boost	V_o	I_g
Buck-Boost	$V_o + V_g$	$I_o + I_g$
Cuk	$V_o + V_g$	$I_o + I_g$
Sepic	$V_o + V_g$	$I_o + I_g$

The equations defined in the table 2 are valid for all the non-isolated converters, with the pole current and throw voltage as defined in table 1. The equations are defined with the turns ratio between L and L_T as 1. The switching transitions are shown in figure 3.

5. Equivalent circuit model

The circuit oriented steady state and dynamic model can be obtained from the idealized analysis, discussed in the above section. Analytical expressions for DC conversion ratio of all topologies may be derived in terms of pole current and throw voltage.

Table 2. Circuit equations governing the sub-intervals for the new family of converters.

Intervals	$i_{La}(t)$	$v_{Ca}(t)$	Time
Interval T_1			
At t_0	0	$V(1+D)$	
$t_o \le t \le t_1$	$\frac{V(1+D)}{L_a}t$	$V(1+D)$	
At t_1	$\frac{I}{2}$	$V(1+D)$	$T_1 = \frac{IL_a}{2V(1+D)}$
Interval T_2			
At t_1	$\frac{I}{2}$	$V(1+D)$	
$t_1 \le t \le t_2$	$V(1+D)\sqrt{\frac{C_a}{L_a}}\sin(\omega t) + \frac{I}{2}$	$V(1+D)\cos(\omega t)$	
At t_2	$2V\sqrt{D}\sqrt{\frac{C_a}{L_a}} + \frac{I}{2}$	$-V(1-D)$	$\omega T_2 = \cos^{-1}\left[\frac{-(1-D)}{(1+D)}\right]$
Interval T_3			
At t_2	$2V\sqrt{D}\sqrt{\frac{C_a}{L_a}} + \frac{I}{2}$	$-V(1-D)$	
$t_2 \le t \le t_3$	$\frac{-V(1-D)}{L_a}t + I_{La}(T_2)$	$-V(1-D)$	
At t_3	0	$-V(1-D)$	$T_3 = \frac{4\sqrt{L_aC_a}\sqrt{D}+IL_a}{2V(1-D)}$

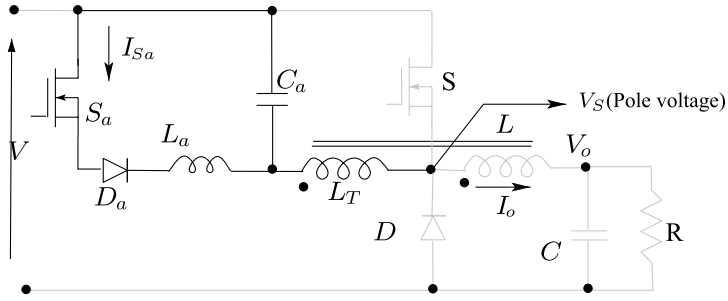


Figure 7. Buck converter with auxiliary circuit.

5.1 *Steady-state equivalent circuit model*

Consider the buck converter shown in figure 7. The conversion ratio $M = V_o/V$ can be evaluated by averaging the pole voltage V_p over a full cycle shown in figure 8. Under the assumption that the resonant frequency is much higher than the switching frequency, the conversion ratio for the buck converter is derived as follows:

$$\frac{V}{T_s}\,(DT_s - T_1 - T_2) \;+\; V\,\frac{T_4}{T_s} = V_o. \tag{3}$$

Assuming the duration T_2 (discharging time of the resonant capacitor) and T_4 (charging time of the resonant capacitor) as equal, we get

$$V\left(D - \frac{T_1}{T_s}\right) = V_o. \tag{4}$$

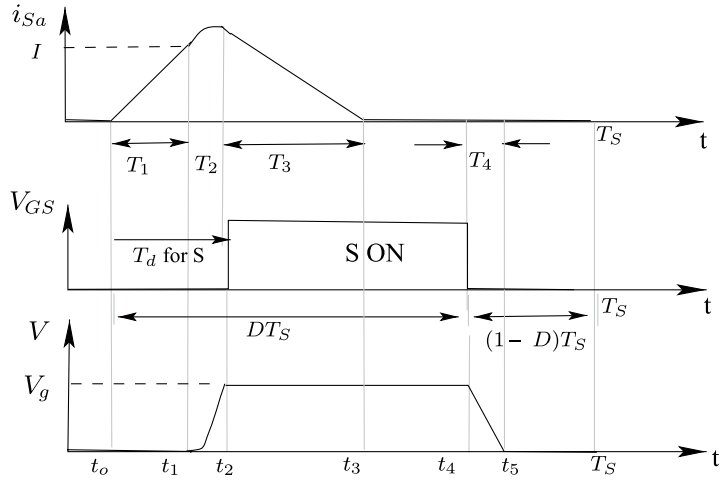


Figure 8. Pole voltage waveforms of buck converter with auxiliary circuit.

From the table 2 defining the circuit equations governing the subintervals for the new family of converters, the interval T_1 is given by (5) i.e.

$$T_1 = \frac{I L_a}{2V(1+D)}. \tag{5}$$

Using eq. 5 in eq. 4 we have

$$\frac{V_o}{V} = D - \frac{I L_a}{2V(1+D)T_s}. \tag{6}$$

We define a normalized current I_N.

$$I_N = \frac{L_a I}{V T_S}. \tag{7}$$

Normalized current is defined in terms of pole current I, throw voltage V, resonant inductor L_a and the switching period T_S given in (7). This will be useful in establishing the performance parameters of the converter.

Eq. 6 may be simplified as

$$\frac{V_o}{V} = D - \frac{I_N}{2(1+D)}. \tag{8}$$

The conversion ratio V_o/V for the buck converter may be simplified as follows.

$$V_o = DV - \frac{L_a}{2(1+D)T_s} I \tag{9}$$

$$V_o = DV - I R_d, \tag{10}$$

where

$$R_d = \frac{L_a}{2(1+D)T_s}. \tag{11}$$

The output voltage exhibits a load dependent drop as seen in eq. 10. This load dependent drop is a function of resonant inductor L_a, duty ratio D and switching period T_s as given in eq. 11. The eq. 10 may be represented by the equivalent circuit as shown in figure 9. The damping resistance R_d is a mathematical artifact to represent the voltage loss on account of delay T_1. There is no energy loss associated with it. The interesting result is that, these converters retain the qualitative nature of the hard switched counterparts with additional lossless damping introduced in the equivalent circuit as shown in figure 9. This simplification

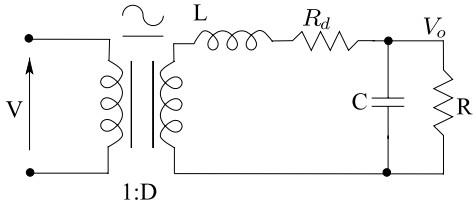


Figure 9. Equivalent circuit of the buck converter with auxiliary circuit.

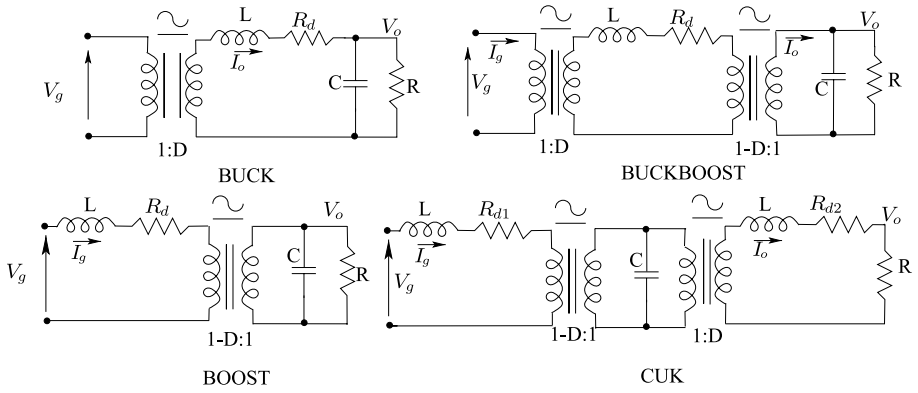


Figure 10. Equivalent circuit model of buck, boost, buck-boost and Cuk converters with auxiliary circuit.

process may be done for all types of converters. The equivalent circuit models for the buck, boost, buckboost and cuk converters are shown in figure 10. Analytical expressions for the equivalent circuit model parameters of boost, buck boost and cuk converters are shown in table 3. In these converters, where the damping is quite substantial, the natural frequencies of the output filter are real; closed loop compensator is easier to design.

5.2 *Small signal equivalent circuit model*

The small signal analysis may be carried out from the equivalent circuit model (Lakshminarasamma & Ramanarayanan 2006; 2007). Consider the equivalent circuit model of buck converter shown in figure 11. Defining the current through the inductor L and the voltage across the capacitor C as the state variables $i(t)$ and $vc(t)$ respectively, the state space averaged equations are given by eq. 12 and eq. 13.

$$L\frac{di(t)}{dt} = Dv - R_d i(t) - v_c(t) \tag{12}$$

$$C\frac{dv_c(t)}{dt} = i(t) + i_z(t) - \frac{v_c(t)}{R}. \tag{13}$$

Table 3. Equivalent circuit model parameters for converters with auxiliary circuit.

Converter	V	I	R_d	$M = V_o/V_g$
Buck	V_g	I_o	$\frac{L_r}{2T_s(1+D)}$	$D - \frac{I_N}{2(1+D)}$
Boost	V_o	I_g	$\frac{L_r}{2T_s(1+D)}$	$\frac{1}{(1-D)+\frac{I_N}{2(1+D)}}$
Buckboost	$V_g + V_o$	$I_o + I_g$	$\frac{L_r}{2T_s(1+D)}$	$\frac{D-\frac{I_N}{2(1+D)}}{(1-D)+\frac{I_N}{2(1+D)}}$
Cuk	$V_g + V_o$	$I_o + I_g$	$R_{d1} = \frac{L_r}{2T_s(1+D)D}$	$\frac{D-\frac{I_N}{2(1+D)}}{(1-D)+\frac{I_N}{2(1+D)}}$
			$R_{d2} = \frac{L_r}{2T_s(1+D)(1-D)}$	

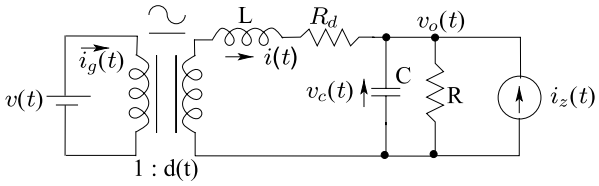


Figure 11. Equivalent circuit model of buck converter with auxiliary circuit.

The average input current for a buck converter is given by the eq. 14.

$$i_g(t) = d(t)i(t). \tag{14}$$

The small signal ac model at a quiescent operating point (I_z,V) is obtained under the assumption, that the input voltage $v(t)$ and the duty cycle $d(t)$ are equal to some given quiescent values V and D, plus some superimposed small ac variations $\hat{v}(t)$ and $\hat{d}(t)$ i.e.

$$v(t) = V + \hat{v}\ ;\ d = D + \hat{d}\ ;\ i_z(t) = \hat{i}_z. \tag{15}$$

In response to these inputs, the average inductor current and the average capacitor voltage will be equal to the corresponding quiescent values I and V_c plus some superimposed small ac variations i.e.

$$i(t) = I + \hat{i} \ \text{ and } \ v_c(t) = V_c + \hat{v}_c. \tag{16}$$

.

With the assumption that the ac variations are small in magnitude compared to the dc quiescent values, i.e.

$$\frac{\hat{v}}{V} \ll 1\ ;\ \frac{\hat{i}}{I} \ll 1\ ;\ \frac{\hat{v}_c}{V_c} \ll 1. \tag{17}$$

The non-linear equations (12), (13) and (14) can be linearalized.

$$\frac{d\hat{i}(t)}{dt} = -\frac{R_d}{L}\,\hat{i} - \frac{1}{L}\,\hat{v}_c + \frac{D}{L}\hat{v} + \frac{V}{L}\,\hat{d} \tag{18}$$

$$\frac{d\hat{v}_c(t)}{dt} = -\frac{1}{C}\,\hat{i} - \frac{1}{RC}\,\hat{v}_c + \frac{1}{C}\,\hat{i}_z. \tag{19}$$

Linearizing the average input current eq. 14, we have

$$\hat{i}_g(t) = D\,\hat{i}(t) + I\,\hat{d}(t) \tag{20}$$

$$\hat{v}(t) = \hat{v}_c. \tag{21}$$

Defining the current through the inductor L and the voltage across the capacitor C as the state variables $i(t)$ and $vc(t)$ respectively, the analytical small signal model has the standard form (derivation shown in § 3) given as:

$$\dot{\hat{x}} = \overbrace{\begin{bmatrix} \frac{-R_d}{L} & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix}}^{A} \overbrace{\begin{bmatrix} \hat{i} \\ \hat{v}_c \end{bmatrix}}^{\hat{x}} + \overbrace{\begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix}}^{b} \hat{v} + \overbrace{\begin{bmatrix} \frac{V}{L} \\ 0 \end{bmatrix}}^{f} \hat{d} + \overbrace{\begin{bmatrix} 0 \\ \frac{1}{C} \end{bmatrix}}^{m} \hat{i}_z \tag{22}$$

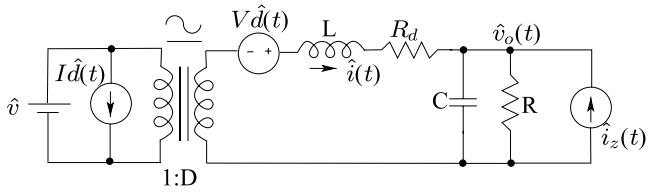


Figure 12. Small signal dynamic model of buck converter with auxiliary circuit.

$$\hat{v}(t) = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i} \\ \hat{v}_c \end{bmatrix} \tag{23}$$

$$\hat{i}_g(t) = D\,\hat{i}(t) + I\,\hat{d}(t). \tag{24}$$

Equivalent circuit model of (22), (23) and (24) is shown in figure 12. Similarly, it is possible to obtain the small signal dynamic models of boost and buck-boost converters.

The interesting result is that, these converters retain the qualitative nature of hard switched counterparts with additional damping introduced in the equivalent circuit as shown in figures 9 and 12. The resonant sub-interval introduces lossless damping to the predominantly second order dynamic model of the converter. This is very similar to the current dependent delay introduced in current programmed converters (Shi-Ping Hsu *et al* 1979).

6. Design validation

Following the guidelines, presented in § 2, 33 Watt auxiliary switch resonant transition boost converter is designed.

6.1 *Specification and design details*

The specifications of the converter are given below.

Input voltage: 18 V to 25 V
Output voltage: 30 V
Output nominal power: 33 Watt
Topology: Non-isolated boost with auxiliary circuit
Controller and strategy: UC494C, duty ratio control with closed loop
Switching frequency: Fixed 400 kHz
Input current ripple: 20%
Output voltage ripple: 1%.

The steps of the design procedure of the power circuit are as follows. Boost converter components; the filter inductor L, main switch S, freewheeling diode D, and the output capacitor C_o are selected using the same procedure as that used for a conventional hard switched boost converter.

6.1a *Main inductor:* The rated current is about 1·43 A. The ripple current is chosen as 0.2 A. With maximum on time of 1 μs, at input voltage of 18 V, this gives an inductor value of approximately 68 μH.

6.1b *Power devices selection:* The power MOSFET has to carry about 2 A and block about 30 V. The diode carries about 1·1 A average current and blocks about 30 V and is suitable for 400 kHz switching. The reverse recovery time has to be better than 50 ns.

6.1c *Output capacitor:* The output capacitor is selected based on the voltage ripple specification. The switching frequency is 400 kHz. This design allows a ripple of 300 mV. Further ESR of the capacitor must be $I_{rms} R_{ESR} \leq 0.3$ i.e. $R_{ESR} = 0{\cdot}4\ \Omega$. The design uses a capacitor 100 μF with ESR of 0·2 Ω.

Auxiliary circuit components; the resonant inductor L_a, resonant capacitor C_a, auxiliary switch S_A and the auxiliary diode D_a form the auxiliary circuit components. The dependent source is generated by a winding L_T coupled to the filter inductor with turns ratio 1.

6.1d *Design of resonant capacitor C_a:* For the present design, with input current $I_g = 1{\cdot}83$ A, output voltage $V = 30$ V, and a current fall time $t_f = 55$ ns for the switching device, the resonant capacitor C_a is selected from eq. 25.

$$C_a = \frac{I_g t_f}{2V} = 2\ \text{nF}. \tag{25}$$

6.1e *Design of resonant inductor L_a:* The resonant interval is assumed to be 5% of the nominal on-time. From the eq. 26, L_a is chosen as 2·2 μH.

$$\frac{\pi}{2}\sqrt{L_a C_a} = 5\%\ of\ T_{on}(\max). \tag{26}$$

6.1f *Selection of the auxiliary switch S_a:* Selection of the auxiliary switch is based on the peak voltage/current stress. Peak voltage stress on the auxiliary switch S_a: $2V_o - V = 42$ V. Peak current stress on the auxiliary switch S_a: $Ig/2 + V_o\sqrt{C_a/L_a} = 2A$.

6.1g *Selection of the auxiliary diode D_a:* Peak voltage and peak current stress on the auxiliary diode are $V = 18$ V and $Ig/2 + V_o\sqrt{C_a/L_a} = 2A$.

Table 4. Components and parameters in the boost converter prototype.

	Components	Parameters
V_g	Input voltage	18–25 V
V_o	Output voltage	30 V
P_o	Output power	33 W
f_s	Switching frequency	400 kHz
L	Input filter	68 μH
C_o	Output filter	100 μF
L_a	Resonant inductor	2 μH
C_a	Resonant capacitor	2 nF
S	Main switch	IRFZ44
D	Main diode	8TQ100
S_a	Auxiliary switch	IRF540
D_a	Auxiliary diode	8TQ100
R	Rated Load	27 Ω

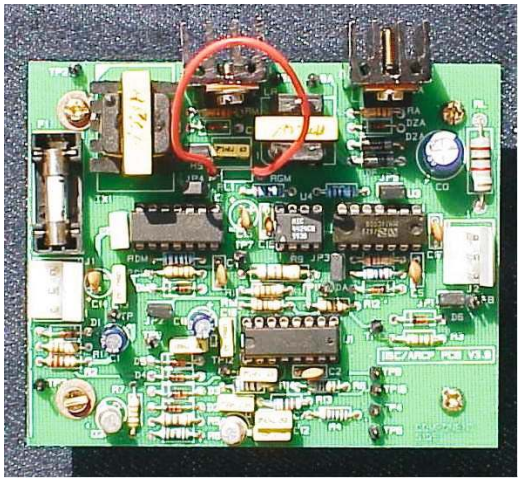


Figure 13. 33 W, 400 kHz boost converter prototype.

7. Experimental results

The steady-state and the transient performance experimental results of the 33 Watt 400 kHz boost converter prototype with auxiliary circuit are presented below.

7.1 *Steady state performance results*

The 33 Watt 400 kHz boost converter prototype with auxiliary circuit is shown in figure 13. Steady state performance results of the 33 Watt 400 kHz boost converter prototype with auxiliary circuit are presented in figure 14.

1. Figure 14(a) shows the gate pulses of frequency 400 kHz driving the auxiliary switch S_a and the main switch S. The main switch is turned-on with a delay after the turn-on of the auxiliary switch.
2. Figure 14(b) shows the pole voltage and the resonant inductor current waveforms. As seen in theoretical waveforms figure 3, there is a linear increase in the resonant inductor current, followed by a resonant interval. Linear resetting of the resonant inductor current to zero follows the resonant interval. This ensures soft turn-off of the auxiliary switch.
3. Figure 14(c) indicates the ZVS turn-on of the main switch. The gate drive is turned-on after the drain-to-source voltage V_{ds} of main switch has reached zero.
4. Figure 14(d) indicates the Zero current switching transitions of the auxiliary switch S_a. The auxiliary switch is turned-on at zero current. After the linear resetting of $i_{sa}(t)$ to zero, the auxiliary switch is turned-off at ZCS.

7.2 *Steady state efficiency results*

The efficiency results of the boost converter at a nominal input voltage of $V = 20$ Volts against load variations from 10% to 100% are presented in table 5. The converter has an efficiency of 92% at full load.

7.2a *Observations:* At low loads, the efficiencies of the hard switched and the soft switched boost converter in the proposed topology are nearly the same. The gain obtained from zero

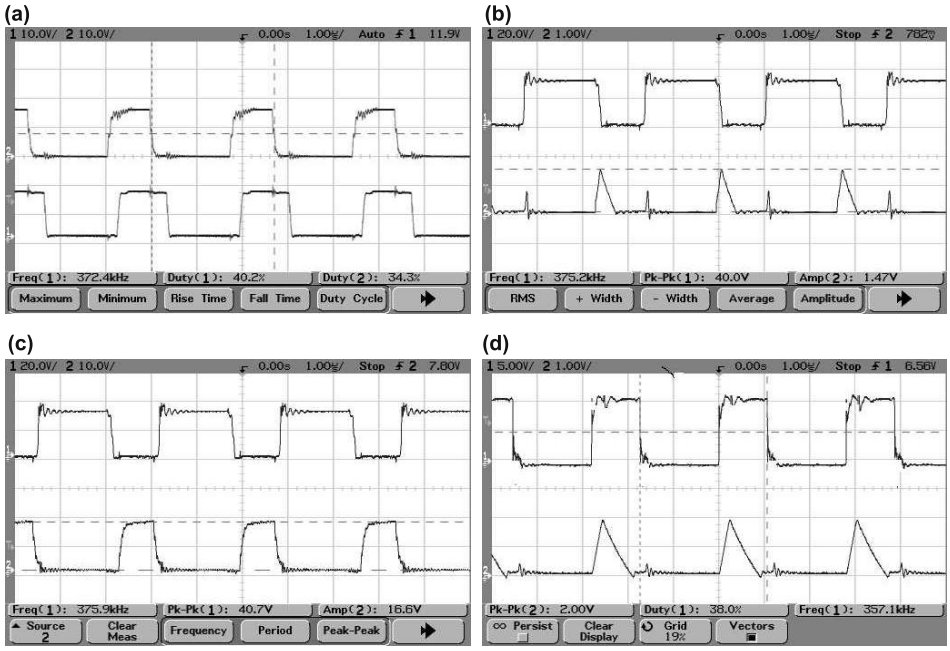


Figure 14. Experimental waveforms of boost converter with auxiliary circuit. **(a)** Ch1: 10 volts/div; Ch2: 10 volts/div: V_{gs} and V_{gsa} of main switch S and the auxiliary switch S_a; **(b)** Ch1: 20 volts/div; Ch2: 1 Amp/div:pole voltage V_p and resonant inductor current $i_{La}(t)$; **(c)** Ch1: 20 volts/div; Ch2: 10 volts/div:V_{ds} and V_{gs} of active switch S indicating ZVS turn-on; **(d)** Ch1: 5 volts/div; Ch2: 1 Amp/div:V_{gsa} and $i_{Sa}(t)$ of auxiliary switch indicating ZCS.

voltage switching in the main switch is lost in the additional loss in the auxiliary switch up to a load of about 20%. Beyond 20% load, there is an improvement in the overall efficiency of the soft switched boost converter. This shows that, the saving of the losses in the main switch is more than the additional losses incurred in the auxiliary circuit. At 60% load, efficiency of 95% is achieved for the soft switched boost converter. There is an efficiency improvement of

Table 5. Steady state efficiency for proposed soft switched boost converter at nominal input voltage for different loads.

Load %	Hard switched (%η)	Soft switched (%η)
10	88	87·83
20	91·22	91·09
30	90·86	92·43
40	88·61	93·33
50	89·09	93·60
60	91·37	94·54
70	90·78	92·53
80	88·29	91·92
100	89·13	91·75

Table 6. Loss comparison for boost converter at $V_g = 20$ V, $V_o = 30$ V, $I_o = 1{\cdot}1$ A, $F_s = 400$ kHz.

Loss Components	Losses (W) Hard switched	Losses (W) Soft switched
Magnetic losses	0·2	0·2
Loss due to ESR of the capacitor	0·05	0·05
Loss due to ESL of the inductor	0·32	0·32
Main circuit		
Power mosfet conduction losses	0·03	0·03
Power mosfet switching losses	2·45	0·09
Freewheeling diode conduction losses	0·59	0·59
Auxiliary circuit		
Auxiliary switch conduction losses	0	0·17
Auxiliary switch switching losses	0	0·28
Auxiliary diode conduction losses	0·59	0·59
Total estimated losses	3·64	2·32
Total measured losses	4·0	2·89

3% from hard switched to soft switched converter. The loss comparison of the hard switched with that of soft switched converter is shown in table 6. The losses due to magnetics, ESR of the output capacitor, ESR of the filter inductor are the same for both the hard switched and the soft switched converters. The switching losses of the converter is constituting the major component of the losses in the hard switched converter. The switching losses of the hard switched converter are nearly 50% of the total measured losses.

8. Small signal model verification of the proposed boost converter

As a means of verification of the small signal model (Middlebrook & Slobodan Cuk 1983) of the soft switched converters, Control to output $\hat{v}_o/\hat{d}$, Output impedance $\hat{v}_o/\hat{i}_o$, Input admittance $\hat{i}_g/\hat{v}$, Audio susceptibility $\hat{v}_o/\hat{v}$ are measured by means of network analyzer for the 33 Watt, 400 kHz boost converter in the proposed topology, operating at 400 kHz with a nominal duty ratio of 0·3 (Lakshminarasamma & Ramanarayanan 2006; 2007).

8.1 *Closed loop results of 33 watt boost converter (proposed topology)*

The control gain characteristics of the hard switched boost converter and the soft switched boost converter results are presented in this section. A comparison of the idealized control gain characteristics of the hard switched boost converter with the measured control gain characteristics of hard switched and soft switched boost converter is performed. Controller is designed and the loop gain characteristics of the soft switched boost converter is presented.

8.1a *Control gain characteristics of hard switched boost converter:* The control gain characteristics of the hard switched boost converter is shown in figure 15. Under nominal operating point, the natural frequency of the converter is in the range of 1141 Hertz to 1579·9 Hertz. The higher frequency is at lower duty ratio. The dc gain from duty ratio to output voltage consists of modulator gain and converter gain. The modulator gain is the reciprocal of the ramp peak in the modulator. In UC494, it is 1/3·5. The converter DC gain is $V_g/(1-d)^2$. The converter

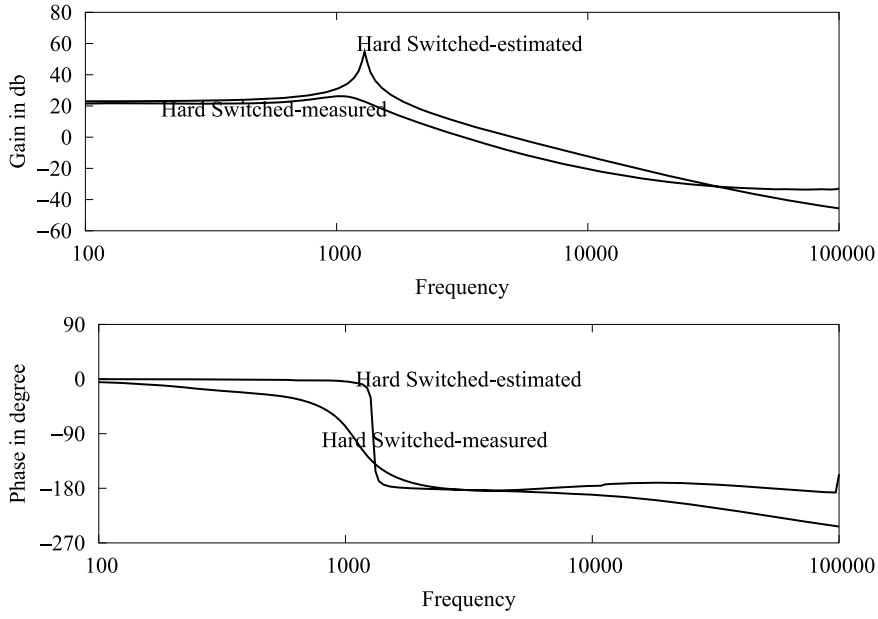


Figure 15. Control gain characteristics of PWM controlled hard switched non-isolated boost converter.

DC gain varies from 50 to 35. The overall gain is therefore 23 dB to 20 dB. The lower gain is at higher input voltage.

8.1b *Control gain characteristics of soft switched boost converter (proposed topology):* Figure 15 shows the control gain characteristics of hard-switched (estimated and measured) and soft switched boost converter control gain results are shown in figure 16. A comparison of the idealized control gain characteristics of the hard-switched with the measured control gain characteristics of hard switched and soft switched boost converter is performed. The idealized control plot of the hard switched boost converter shows underdamped behaviour. The measured control gain of the hard-switched boost converter exhibits damping as observed in the plot. This is on account of the on-state loss of the main switch, loss in parasitics of the circuit like winding resistance of filter inductor L, etc. The damping exhibited by the hard-switched boost converter is lossy.

The damping exhibited by the soft switched converter is due to the resistance R_d as seen from the equivalent circuit model in figure 10. From the eq. 11, this damping resistance R_d is a function of resonant inductor L_r, switching period T_s and duty ratio. The damping resistance R_d is a mathematical artifact to represent the voltage loss on account of the delay T_1. There is no energy loss associated with it. The damping is substantial so that the characteristic frequencies are real.

The gain plot exhibits substantial damping so that the characteristic frequencies are real (f_{p1}, f_{p2} indicated in figure 16). The effect of left half plane zero f_{z1} - ESR of the capacitor and right half plane zero f_{z2} - inherent in the boost converter is observed in gain plot figure 16.

8.1c *Controller design—Soft switched boost converter:* The controller used is a PI controller with lead/lag compensator. The PI corner frequency is chosen at 1141 Hz. The lead/lag com-

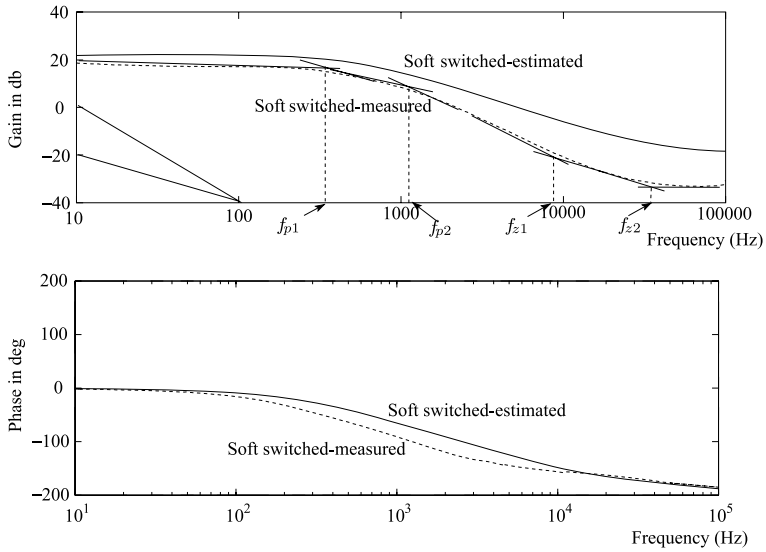


Figure 16. Control gain characteristics of soft switched non-isolated boost converter.

pensator frequencies are chosen as 1141 Hz and 11410 Hz. The dc feedback gain is [30/11]. The loop-gain cross-over frequency is 3 kHz at $V_g = 22$ V and duty ratio $D = 0{\cdot}3$ as observed in loop gain plot figure 17.

Control to output $\hat{v}_o/\hat{d}$, output impedance $\hat{v}_o/\hat{i}_o$, input admittance $\hat{i}_g/\hat{v}$, audio susceptibility $\hat{v}_o/\hat{v}$ measurements are done with the auxiliary circuit disabled (hard switched boost

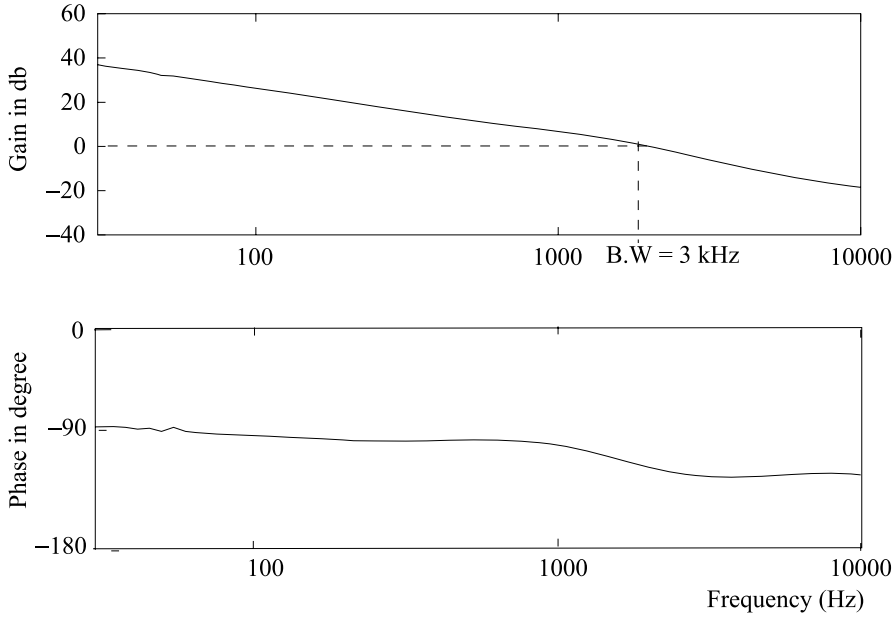
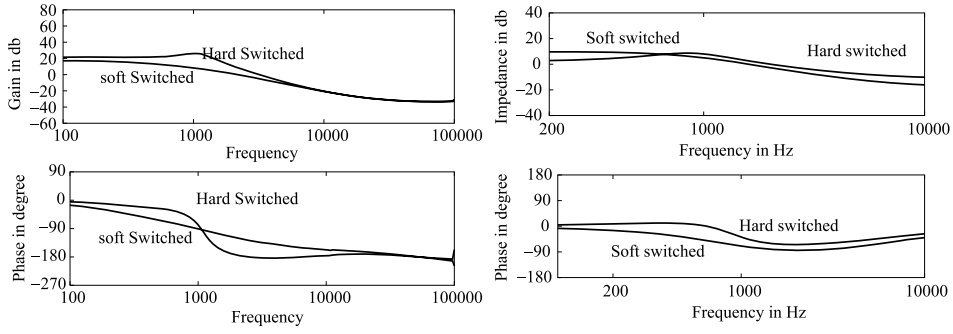


Figure 17. Loop gain characteristics of soft switched non-isolated boost converter.



(a) Control gain characteristics (b) Output impedance characteristics

Figure 18. Control gain and output impedance plots of hard-switched and soft switched boost converter.

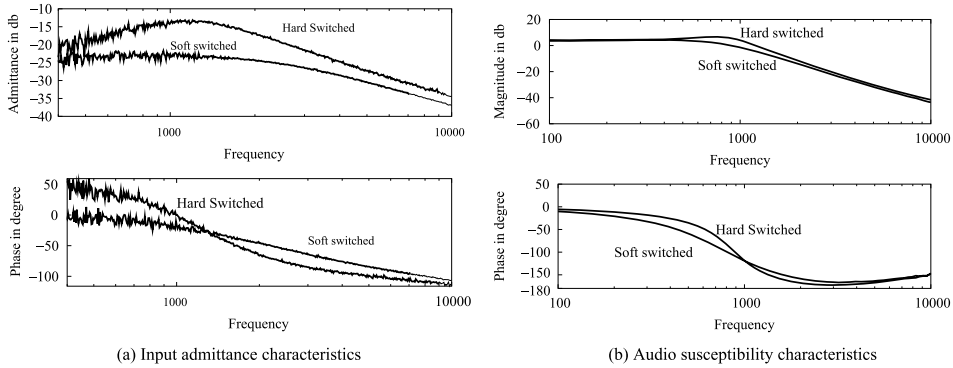
converter) and the auxiliary circuit enabled (soft switched boost converter) for the 33 Watt, 400 kHz boost converter prototype.

Figures 18 and 19 show the magnitude and phase plot of control to output, output impedance, input admittance, audio susceptibility transfer functions of the hard switched boost converter and the soft switched boost converter (Lakshminarasamma & Ramanarayanan 2006; 2007). In all these functions, it may be observed that the lossless damping introduced by the resonant switching process has made the LC filter poles real.

9. Conclusion

This paper presented the design methodology for the new family of soft transition converters; the design guidelines and methodology of design of these converters were presented through an example.

This family of converters were analysed in terms of the pole current and throw voltage, the defining equations of all converters belonging to this family become identical. A simple circuit oriented model emerged from such a description. This paper presented the dynamic



(a) Input admittance characteristics (b) Audio susceptibility characteristics

Figure 19. Input admittance and Audio susceptibility plots of hard-switched and soft switched boost converter.

models for the family of auxiliary switch resonant transition converters. Steady state and dynamic performance results of the 33 Watt 400 kHz auxiliary switch resonant transition boost converter prototype were presented.

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Notations

S	Main switch
S_a	Auxiliary switch
D	Main diode
D_a	Auxiliary diode
L_a	Resonant inductor
C_a	Resonant capacitor
V_T	Throw voltage
I_P	Pole current
I_g	Input current
f_S	Switching frequency
$i_{La}(t)$	Resonant inductor current
$i_{Sa}(t)$	Auxiliary switch current
$v_{Ca}(t)$	Resonant capacitor voltage
V_o	Output voltage
V_g	Input voltage
V_S	Voltage across the main switch
I_S	Current through the main switch

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